74LVC1G79

Single D-type flip-flop; positive-edge trigger; synchronous reset active low

Rev. 07 — 29 August 2007 Product data sheet

1. General description

The 74LVC1G79 provides a single positive-edge triggered D-type flip-flop.

Information on the data input is transferred to the Q-output on the LOW-to-HIGH transition of the clock pulse. The D-input must be stable one set-up time prior to the LOW-to-HIGH clock transition for predictable operation.

Inputs can be driven from either 3.3 V or 5 V devices. This feature allows the use of this device in a mixed 3.3 V and 5 V environment.

This device is fully specified for partial power-down applications using I_{OFF}. The I_{OFF} circuitry disables the output, preventing the damaging backflow current through the device when it is powered down.

5. Functional diagram

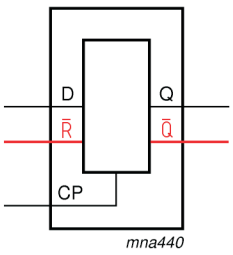

Fig 1. Logic symbol

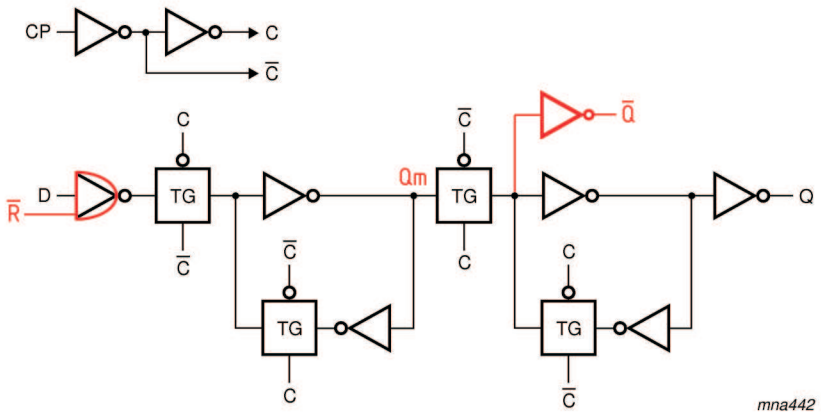

Fig 3. Logic diagram

NODE DESCRIPTION
D : data input
$\overline{R}$: reset input
CP : clock pulse input
C : clock
$\overline{C}$: complementary clock
Qm : master latch output
Q : data output
$\overline{Q}$: complementary data output

7. Functional description

Table 4. Function table[1]

Input			Output	
CP	$\overline{R}$	D	Q	$\overline{Q}$
↑	H	L	L	H
↑	H	H	H	L
L, H, ↓	X	X	q	$\overline{q}$
↑	L	X	L	H

[1] H = HIGH voltage level;
L = LOW voltage level;
↑ = LOW-to-HIGH CP transition;
X = don't care;
q = lower case letter indicates the state of referenced input, one set-up time prior to the LOW-to-HIGH CP transition.