II	III	IV	V	VI
	B	C	N	
	Al	Si	P	S
Zn	Ga	Ge	As	Se
Cd	In	Sn	Sb	Te

2.33 28.086

Si

5.43 14

$3s^2 3p^2$

1683 DIA 625

Silicon (Si) – the dominating material in IC manufacturing

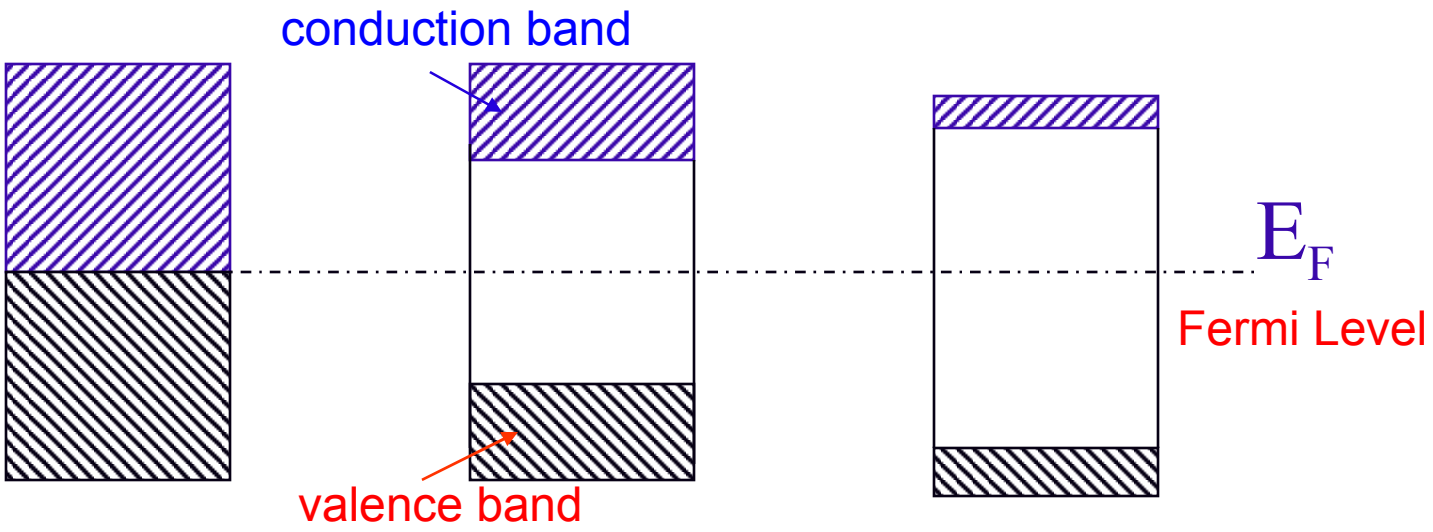
Compound semiconductors

III - V group:

- **GaAs**
- **GaN**
- **GaSb**
- **GaP**
- **InAs**
- **InP**
- **InSb**

.....

The Energy Band Structure



conductor

semiconductor
Eg~0.16 aJ

insulator
Eg~1.6 aJ

Material	Electrical conductivity σ
Metal	$\sigma > 10^5\ \Omega^{-1}m^{-1}$
Semiconductor	$10^5\ \Omega^{-1}m^{-1} > \sigma > 10^{-8}\ \Omega^{-1}m^{-1}$
Insulator	$\sigma < 10^{-8}\ \Omega^{-1}m^{-1}$

Controlling Conductivity

$$\sigma = qn\mu$$

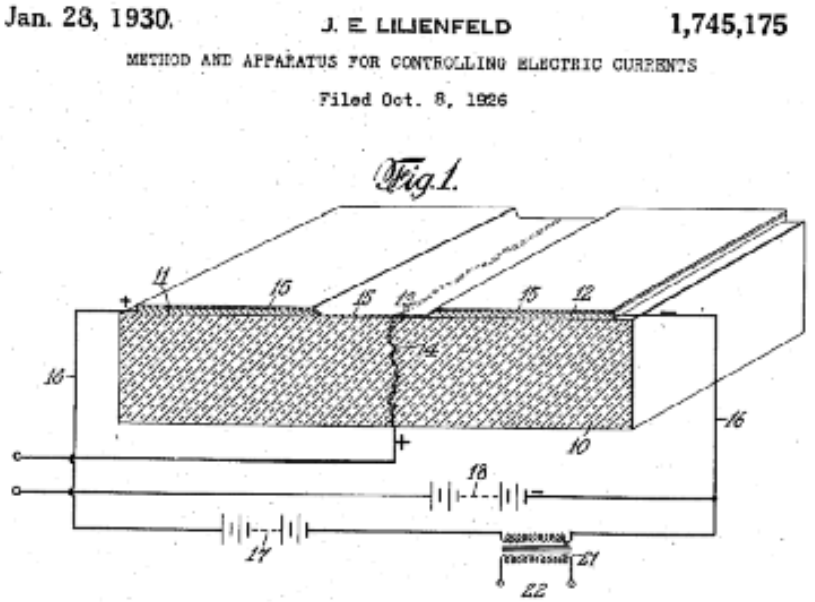
MOS Transistor

transfer re**sistor**

1930 J. Lilienfend applied for a patent regarding a field-effect device in USA

1935 O. Heil - similar patent in UK

1960 Practical manufacturing of a field-effect transistor


Jan. 28, 1930. J. E. LILIENFELD 1,745,175

METHOD AND APPARATUS FOR CONTROLLING ELECTRIC CURRENTS

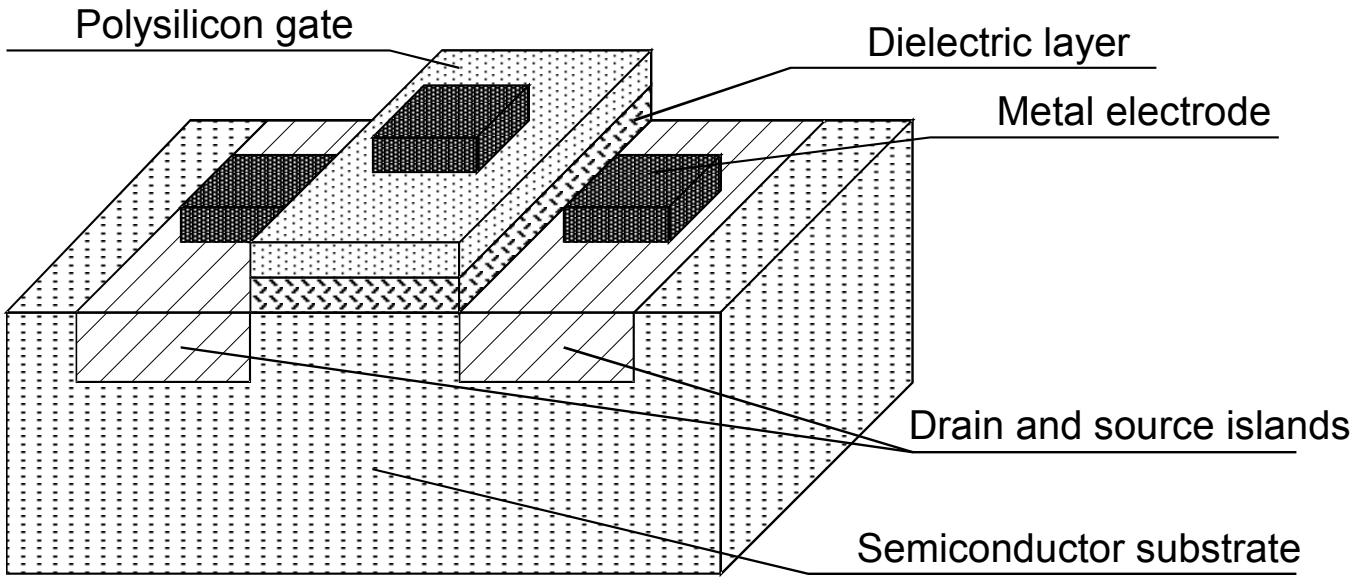
Filed Oct. 8, 1926

Fig. 1.

MOS Transistor

Metal Oxide Semiconductor

Various names: MOSFET, MIS, IGFET

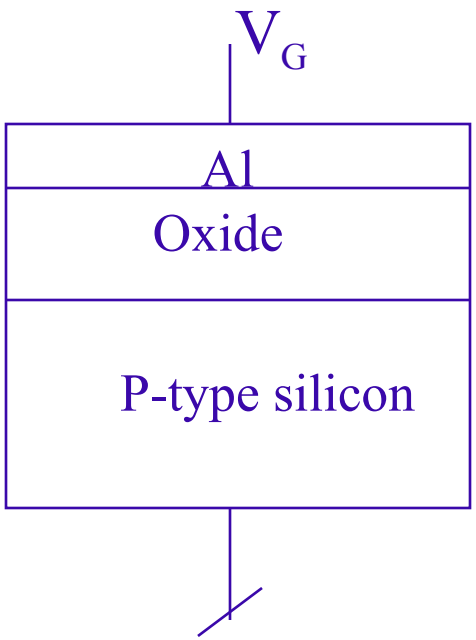


ρ of the substrate: 0.01 - 0.1 Ωm

n+ concentration: 10^{24} - 10^{26} m^{-3}

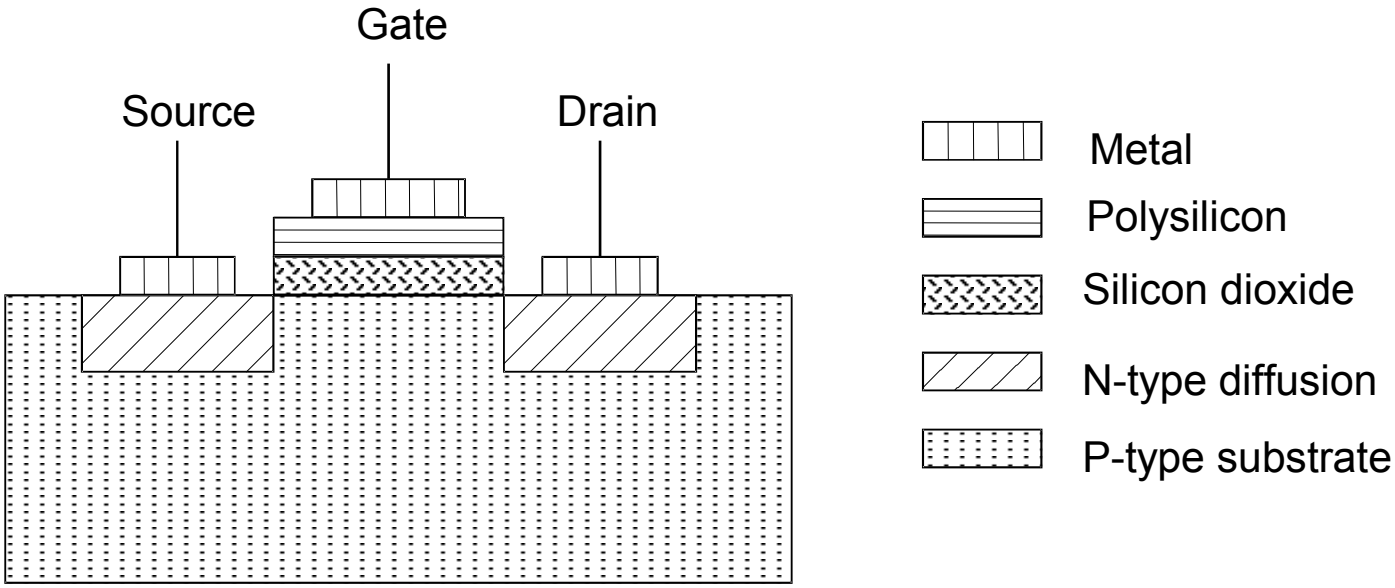
$t_{ox:}$: 1-100 nm

The MOS Capacitor



- Accumulation $V_G<0$
- Depletion $V_G>0$
- Inversion $V_G>>0$

nMOS Cross-section

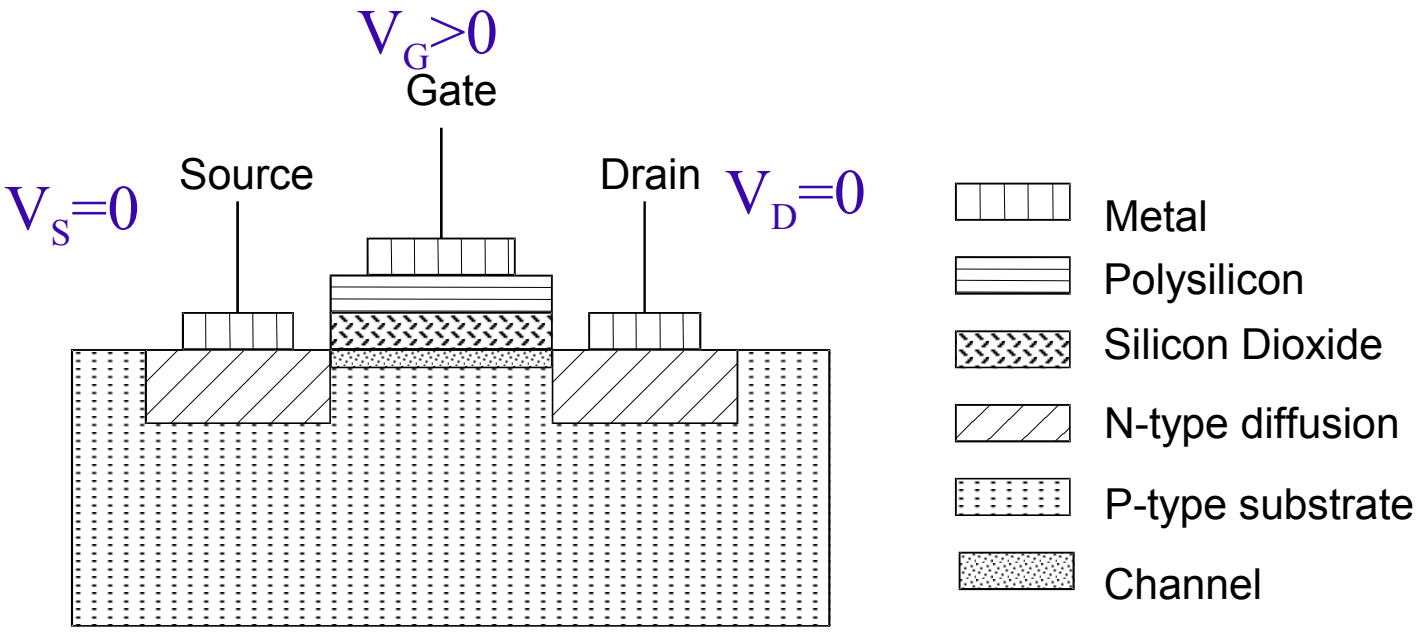


Classification of MOS Transistors

N-channel
P-channel

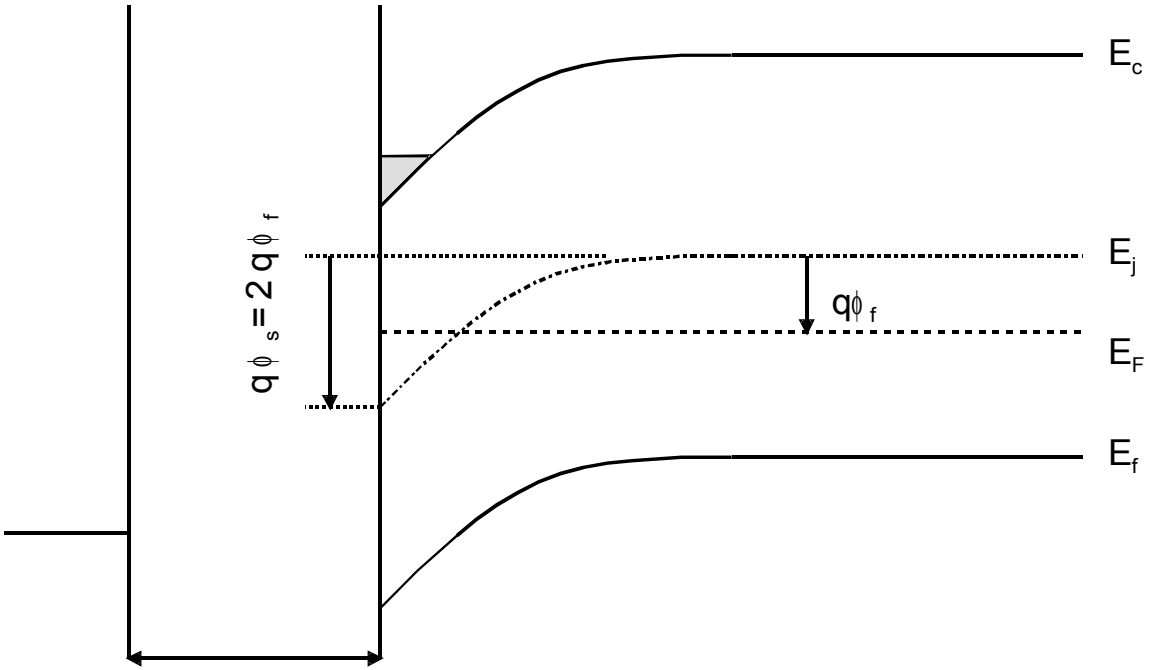
Depletion mode
Enhancement mode

nMOS Transistor with Biased Gate

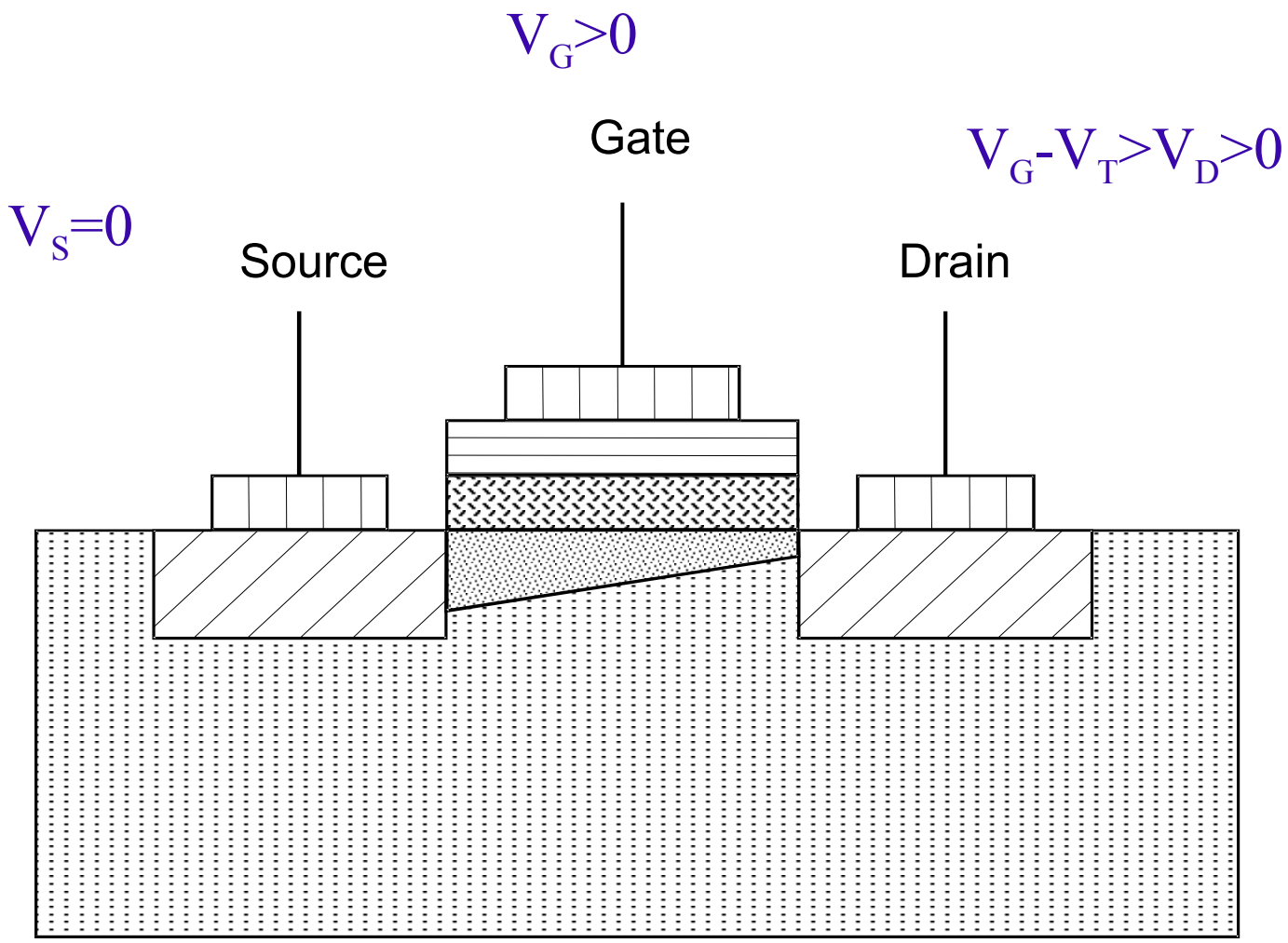


Beginning of The Strong Inversion

$$V_G = V_T$$

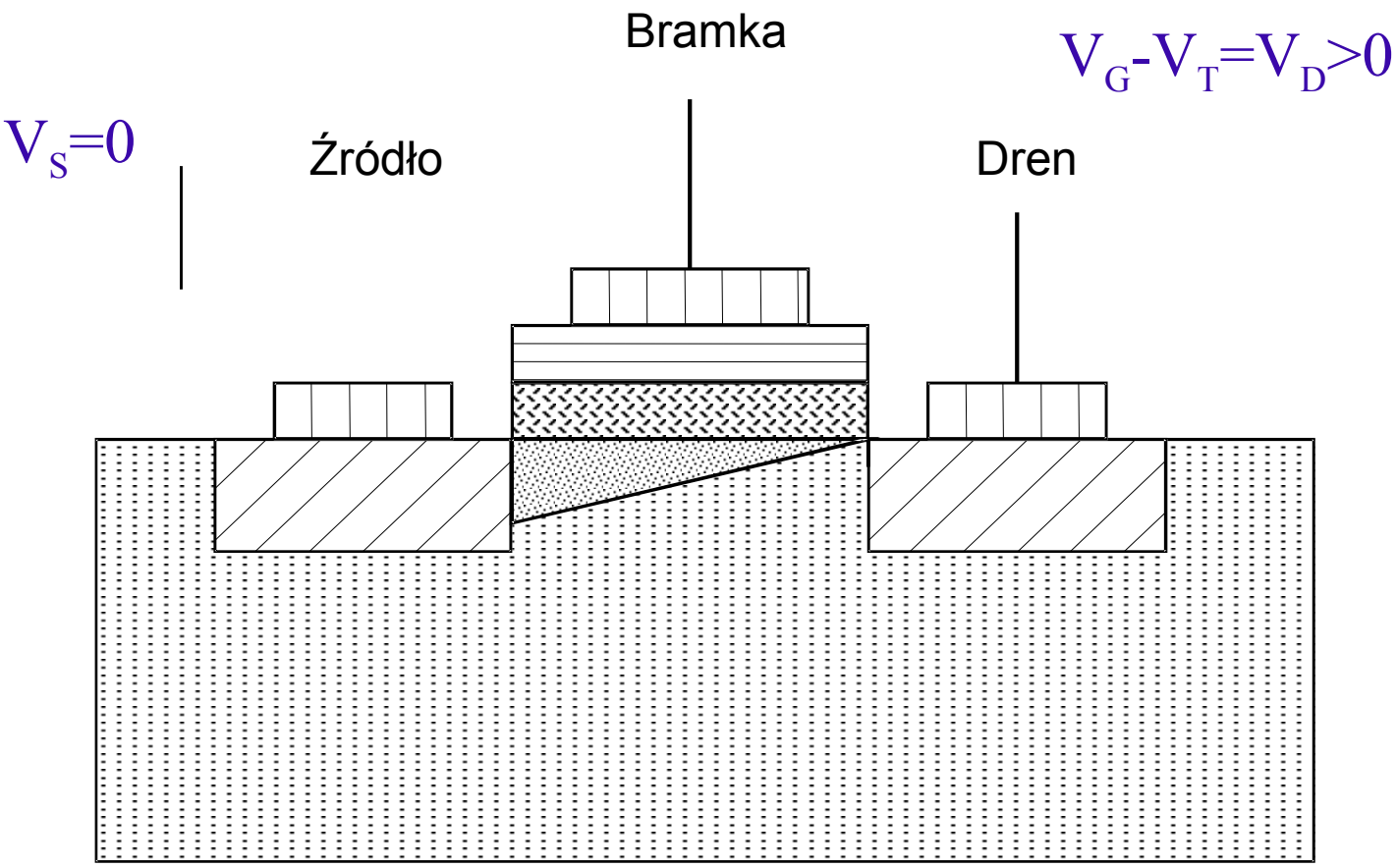


Conducting nMOS Transistor

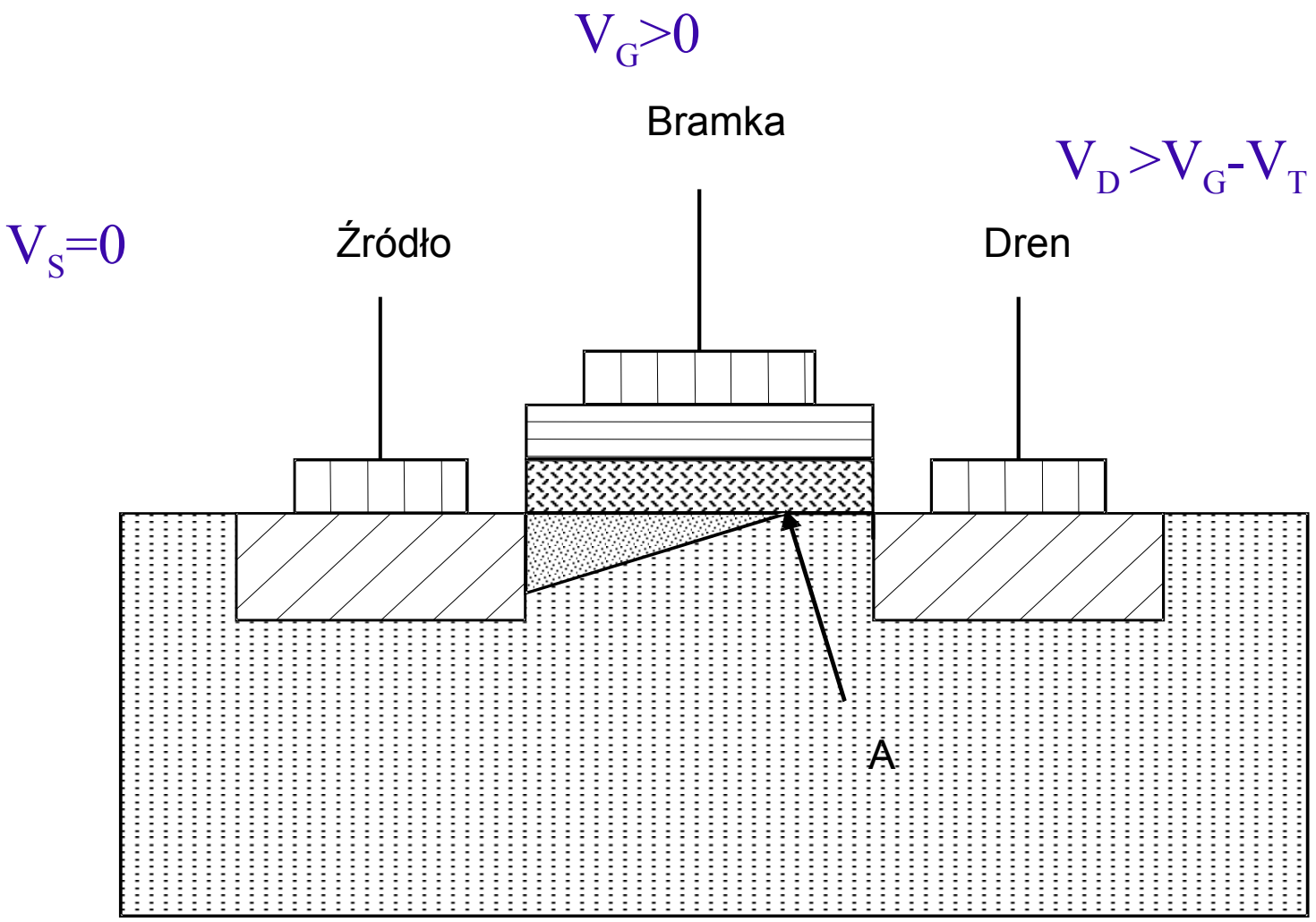


Conducting nMOS at The Beginning of Saturation

$V_G>0$



Saturated nMOS Transistor



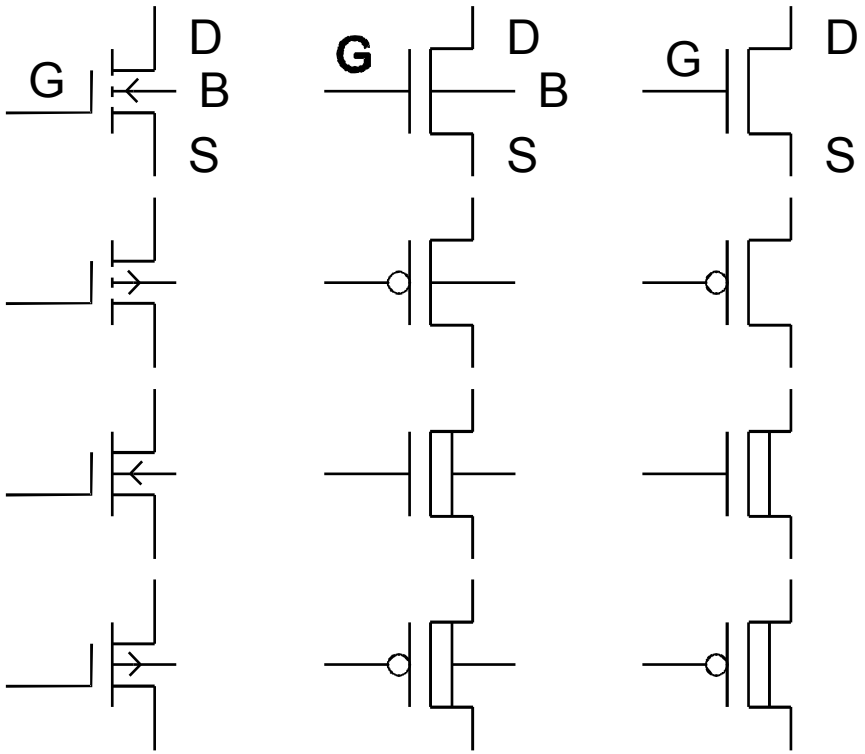
MOS Symbols

N-type enhancement mode

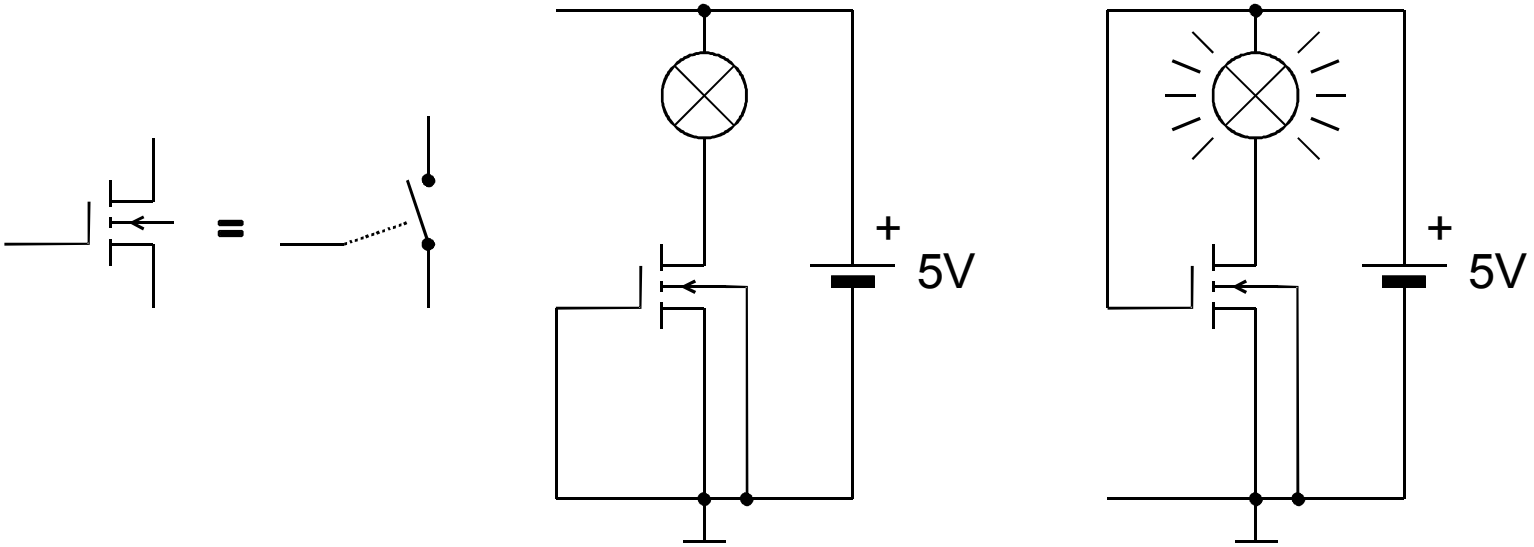
P-type enhancement mode

N-type depletion mode

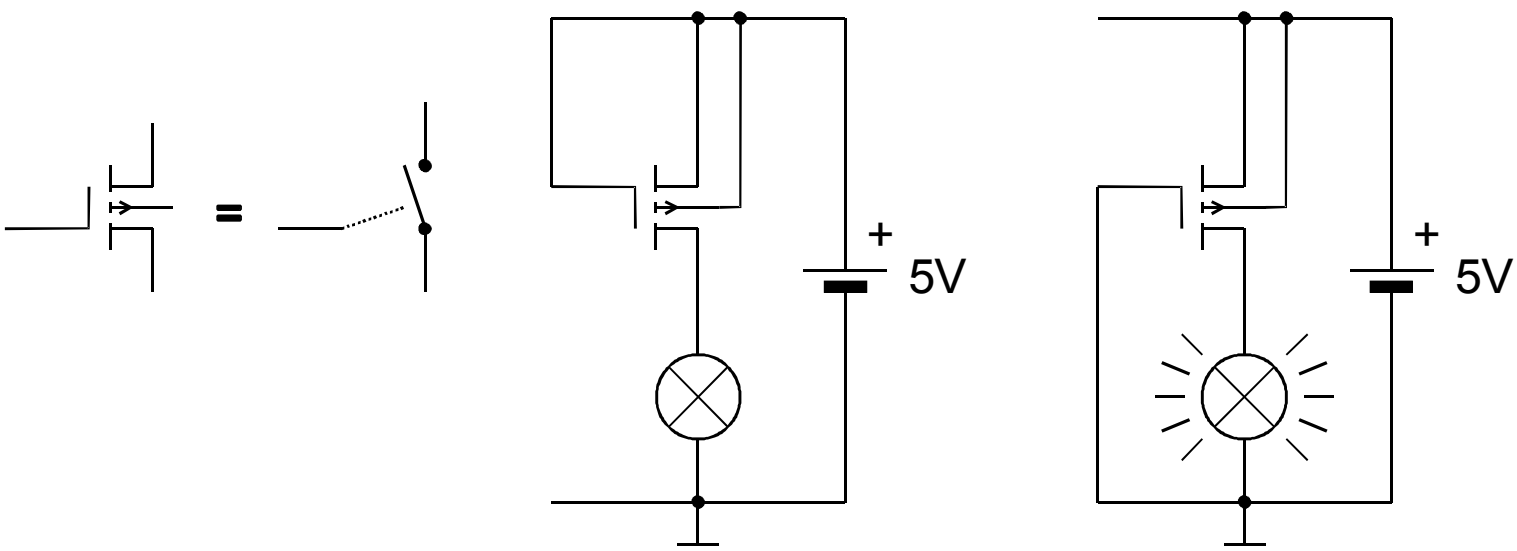
P-type depletion mode



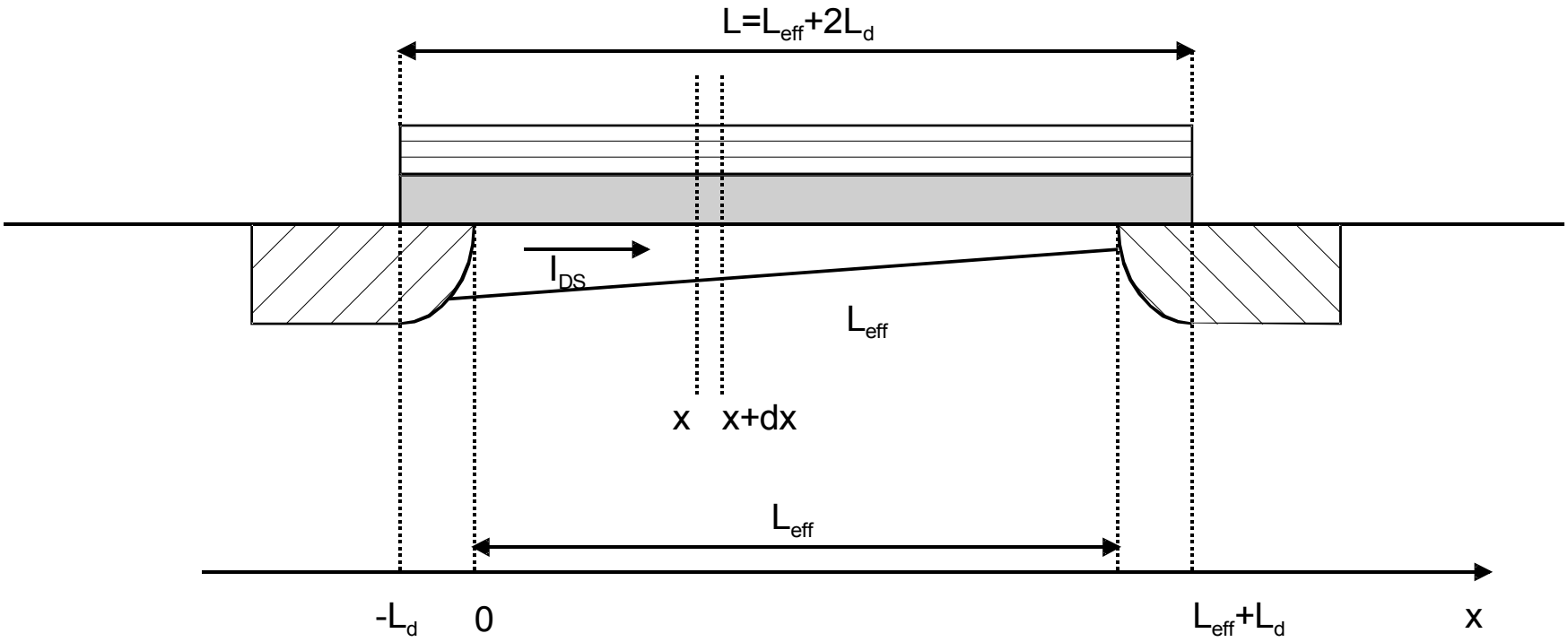
nMOS as A Switch



pMOS as A Switch



MOS in Linear Range



$$I_{DS} = \mu \frac{W_{eff}}{L_{eff}} C_{ox} \int_0^{U_{DS}} (U_{GS} - V_{T0} - V(x))\,dV$$

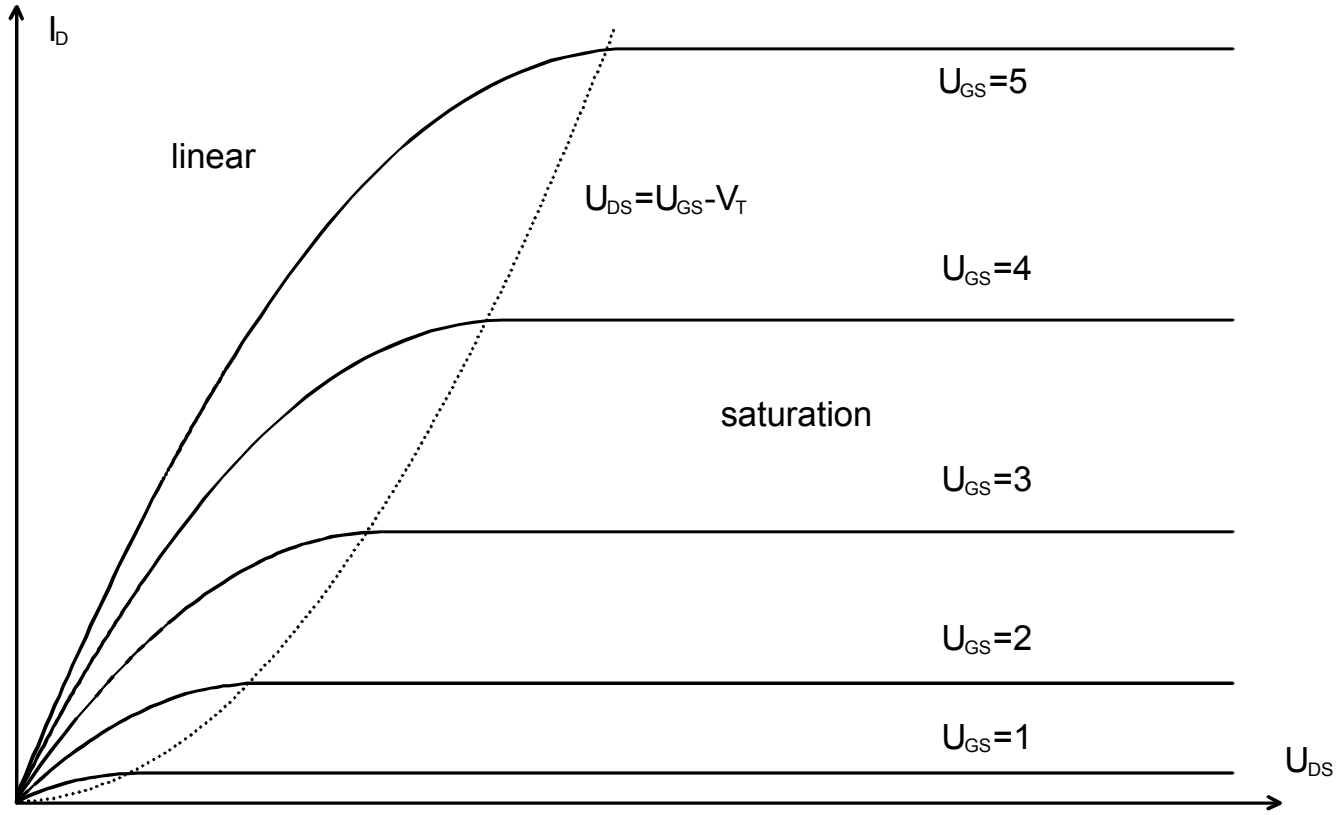
$$I_{DS} = \mu \frac{W_{eff}}{L_{eff}} C_{ox} \left((U_{GS} - V_{T0}) U_{DS} - \tfrac{1}{2} U_{DS}^2 \right)$$

$$I_{DS} = k_p \frac{W_{eff}}{L_{eff}} \left((U_{GS} - V_{T0}) U_{DS} - \tfrac{1}{2} U_{DS}^2 \right) \qquad \text{Linear}$$

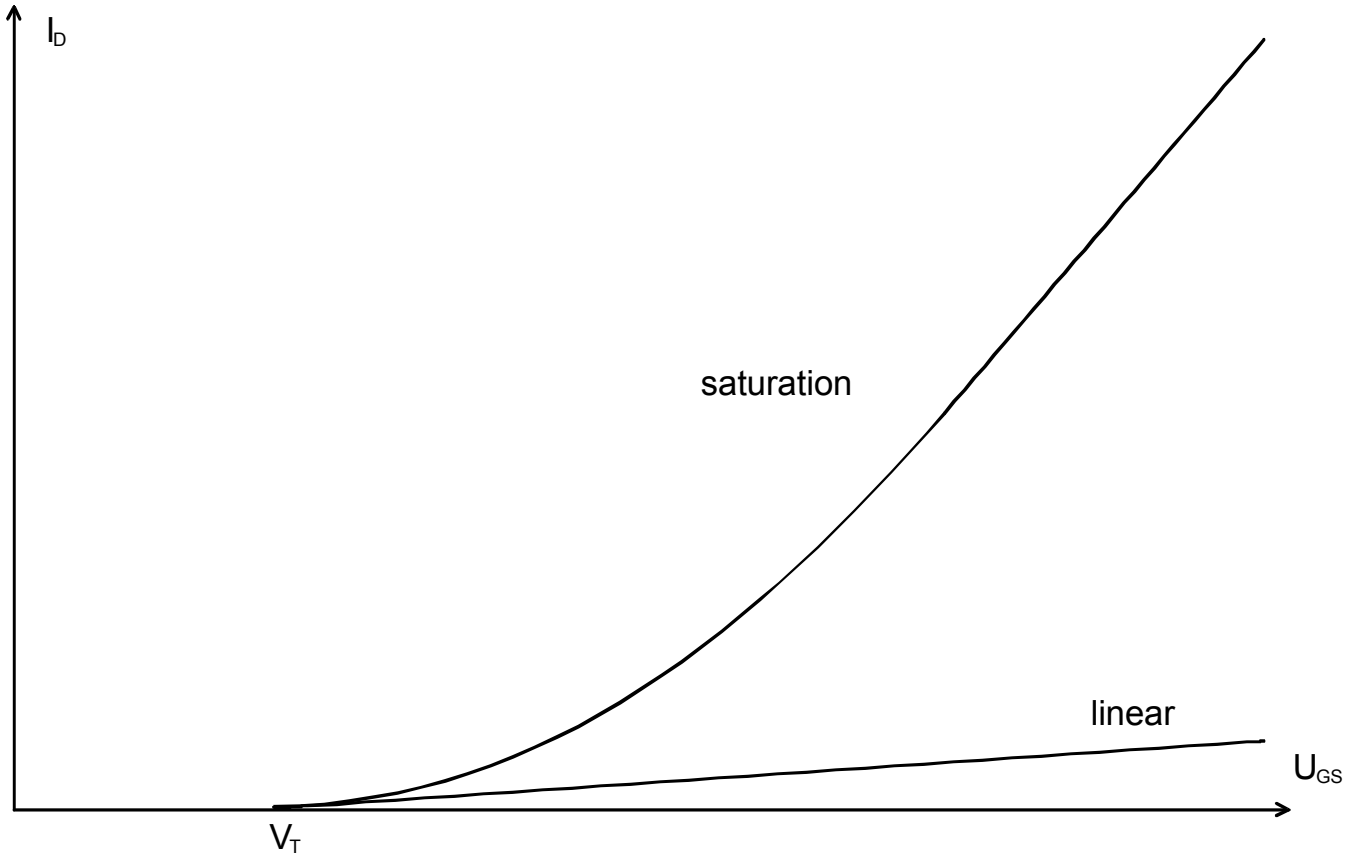
$$I_{DS} = \frac{k_p}{2} \frac{W_{eff}}{L_{eff}} (U_{GS} - V_{T0})^2 \qquad \text{Saturation}$$

$\beta = \mu\varepsilon/t_{ox}(W/L)$ Transistor gain factor

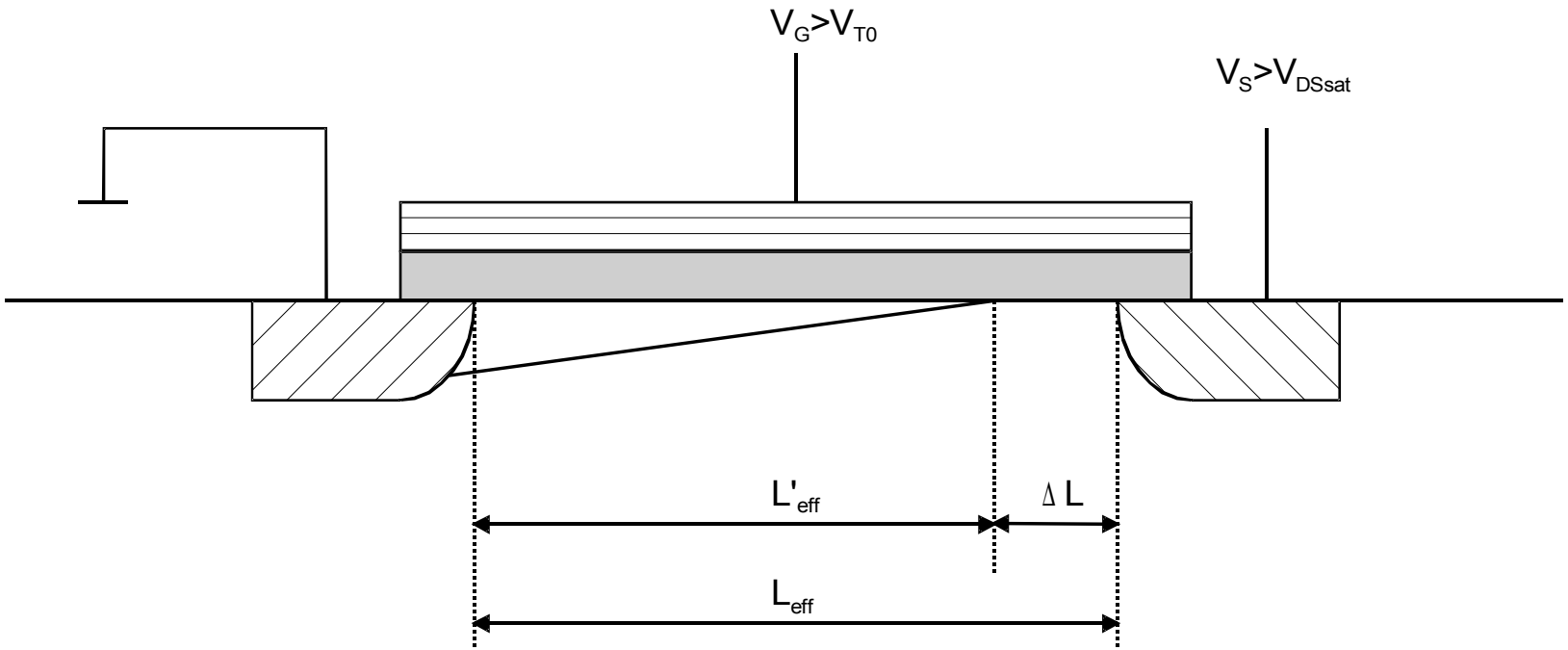
MOS Output Characteristics



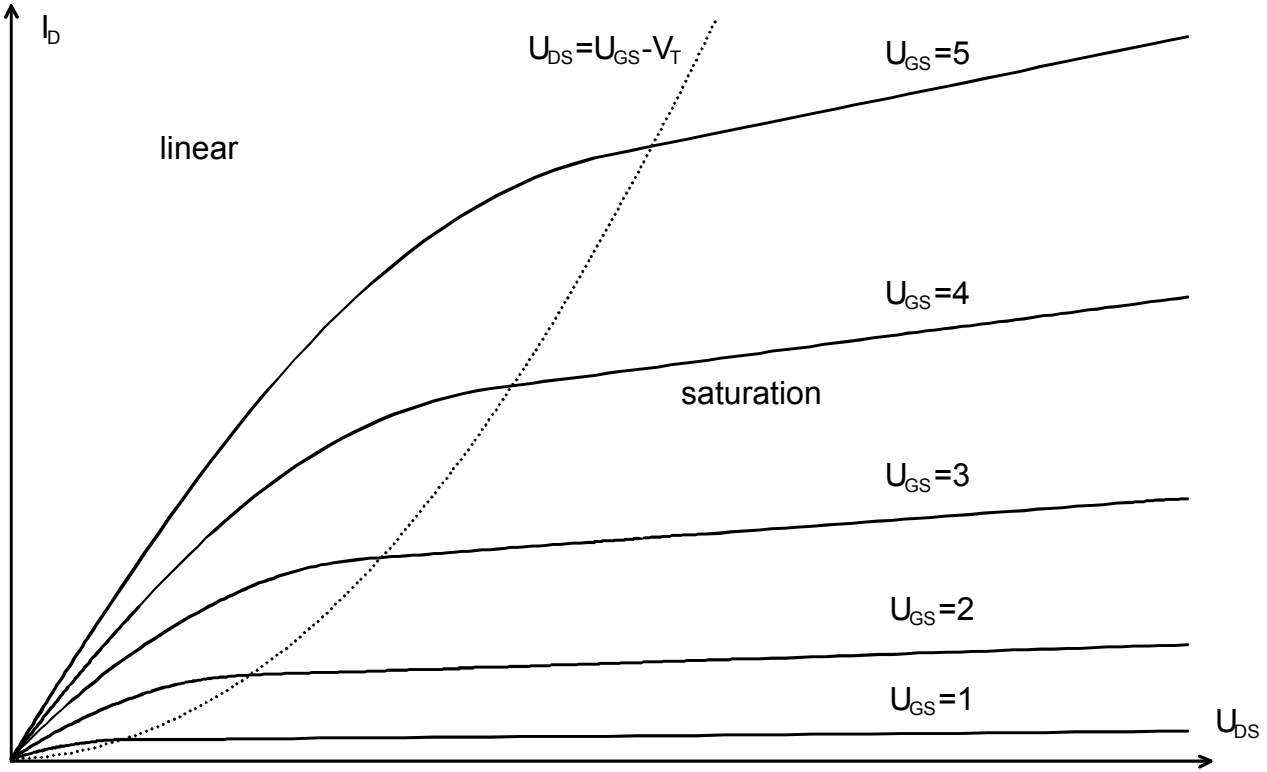
MOS Transfer Characteristics



Channel Length Modulation



Model LEVEL1



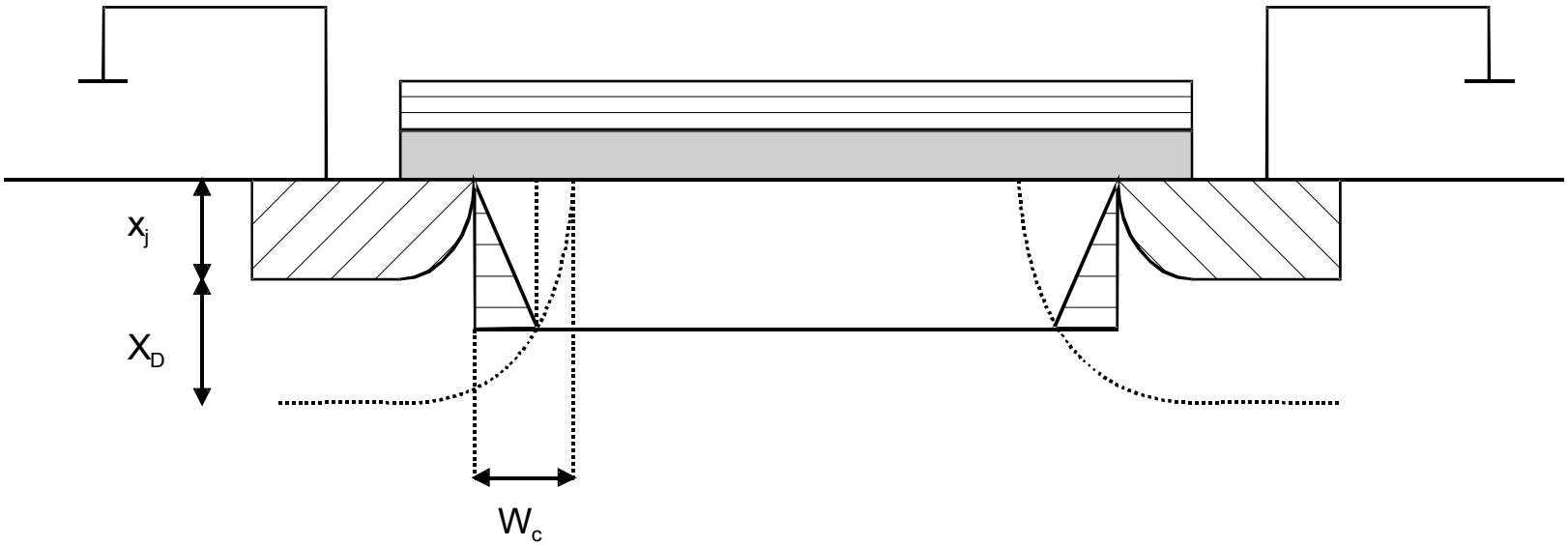
SPICE DC Parameters for 1μm MOS

Parameter	nMOS	pMOS	Units	Description
VTO	0.7	0.7	volt	Threshold voltage
KP	$8*10^{-5}$	$2.5*10^{-5}$	A/V^2	Transconductance coefficient
GAMMA	0.4	0.5	$V^{0.5}$	Bulk threshold parameter
PHI	0.37	0.36	volt	Surface potential at strong inversion
LAMBDA	0.01	0.01	$volt^{-1}$	Channel length modulation parameter
LD	$0.1*10^{-6}$	$0.1*10^{-6}$	meter	Lateral diffusion
TOX	$2*10^{-8}$	$2*10^{-8}$	meter	Oxide thickness
NSUB	$2*10^{16}$	$4*10^{16}$	$1/cm^3$	Substrate doping density

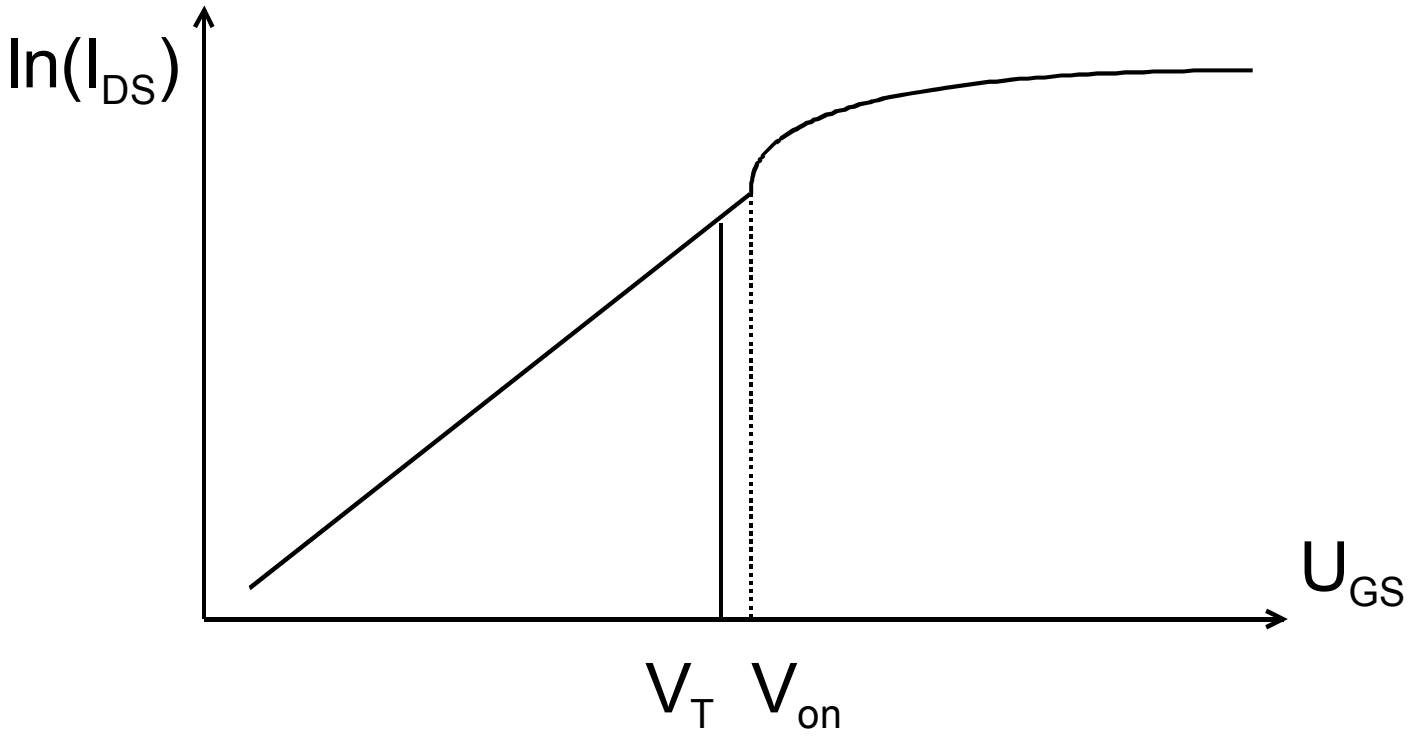
What's new in LEVEL3

- Modified threshold voltage model, taking into account the drain induced barrier lowering (DIBL)
- Longitudinal and transversal electric field dependent mobility model
- Improved channel length modulation and saturation voltage model
- Weak inversion (subthreshold) range

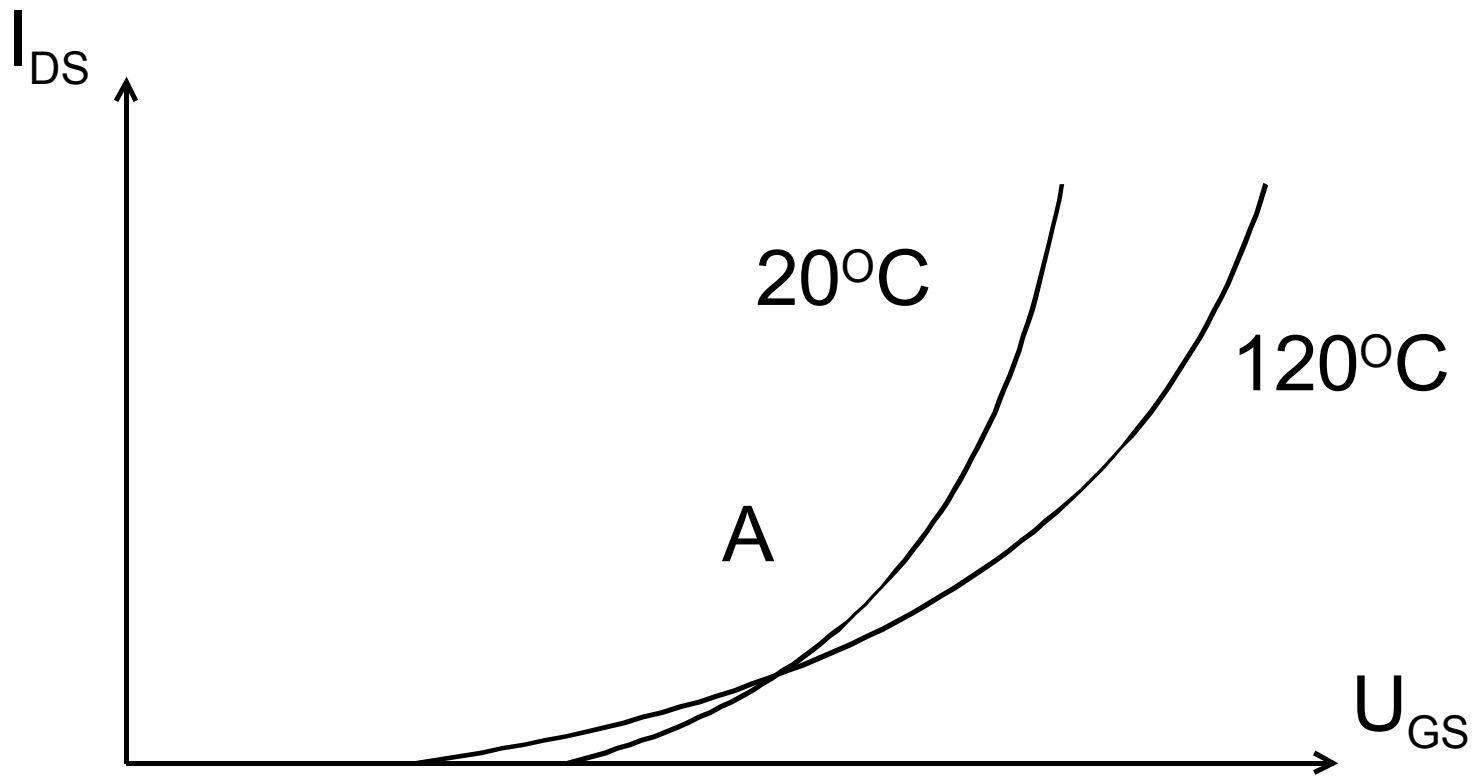
Trapezoidal Charge Approximation



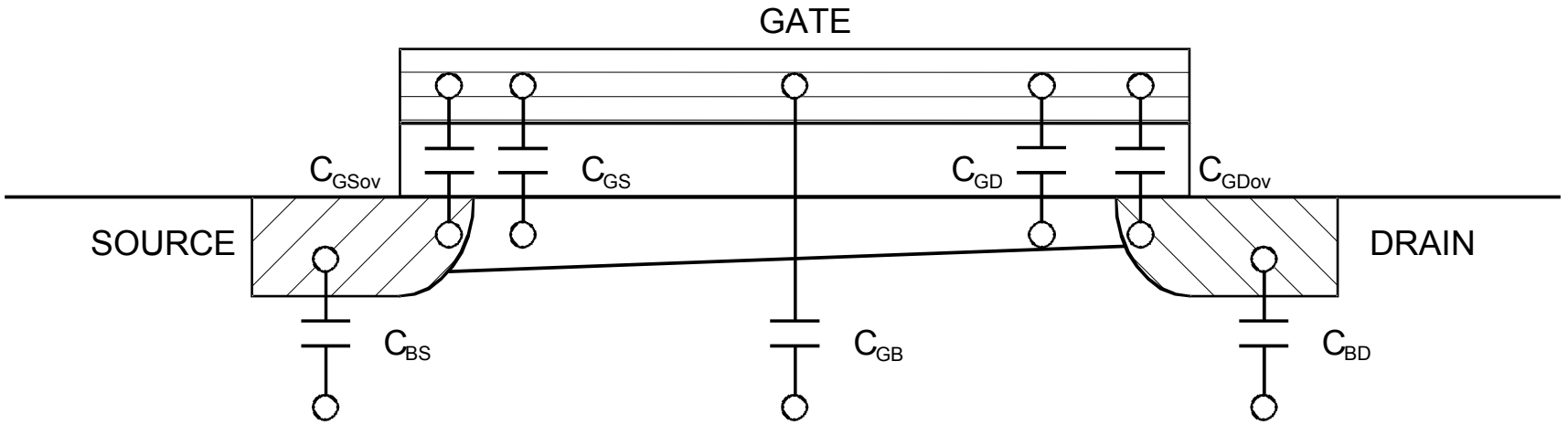
Subthreshold Range



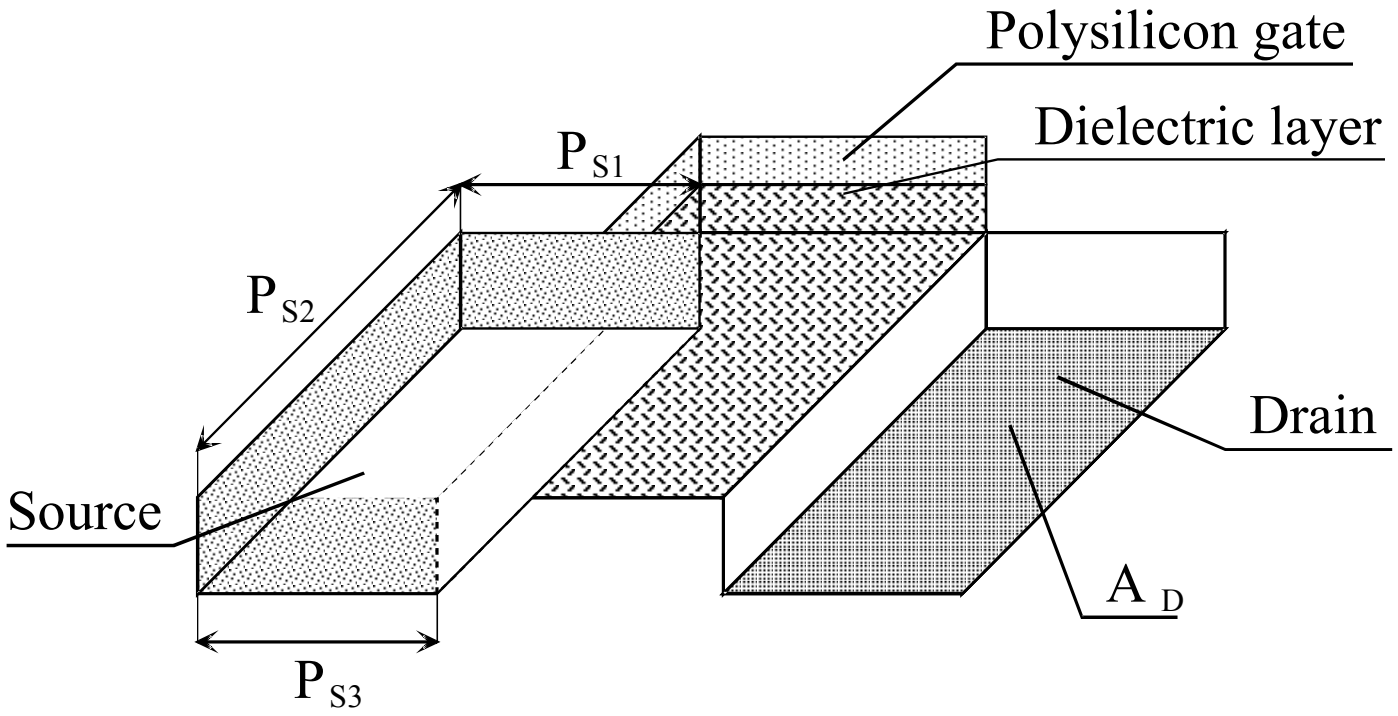
Temperature Influence on MOS Characteristics



MOS Capacitances



MOS Capacitancies



MOS Capacitances

$$C_{BD} = \frac{C_j A_D}{\left(1 - \frac{U_{BD}}{\phi_j}\right)^{M_j}} + \frac{C_{jsw} P_D}{\left(1 - \frac{U_{BD}}{\phi_j}\right)^{M_{jsw}}}$$

$$C_{BS} = \frac{C_j A_S}{\left(1 - \frac{U_{BS}}{\phi_j}\right)^{M_j}} + \frac{C_{jsw} P_S}{\left(1 - \frac{U_{BS}}{\phi_j}\right)^{M_{jsw}}}$$

$$C_{GDov} = C_{GDO} W_{eff}$$

$$C_{GSov} = C_{GSO} W_{eff}$$

$$C_{GSO} = C_{GDO} = C_{ox} L_d$$

Accumulation

$$C_{GB} = C_{ox} W_{eff} L_{eff}$$

Depletion

$$C_{GB} = \frac{C_{ox} W_{eff} L_{eff}}{\sqrt{1 + 4\left(\frac{U_{GB} - U_{FB}}{\gamma^2}\right)}}$$

MOS Capacitances

Linear range ($C_{GB} = 0$)

$$C_{GS} = \frac{2}{3} C_{ox} W_{eff} L_{eff} \left(1 - \frac{(U_{GS} - U_T)^2}{(U_{GS} - U_T + U_{GD} - U_T)^2} \right)$$

$$C_{GD} = \frac{2}{3} C_{ox} W_{eff} L_{eff} \left(1 - \frac{(U_{GD} - U_T)^2}{(U_{GS} - U_T + U_{GD} - U_T)^2} \right)$$

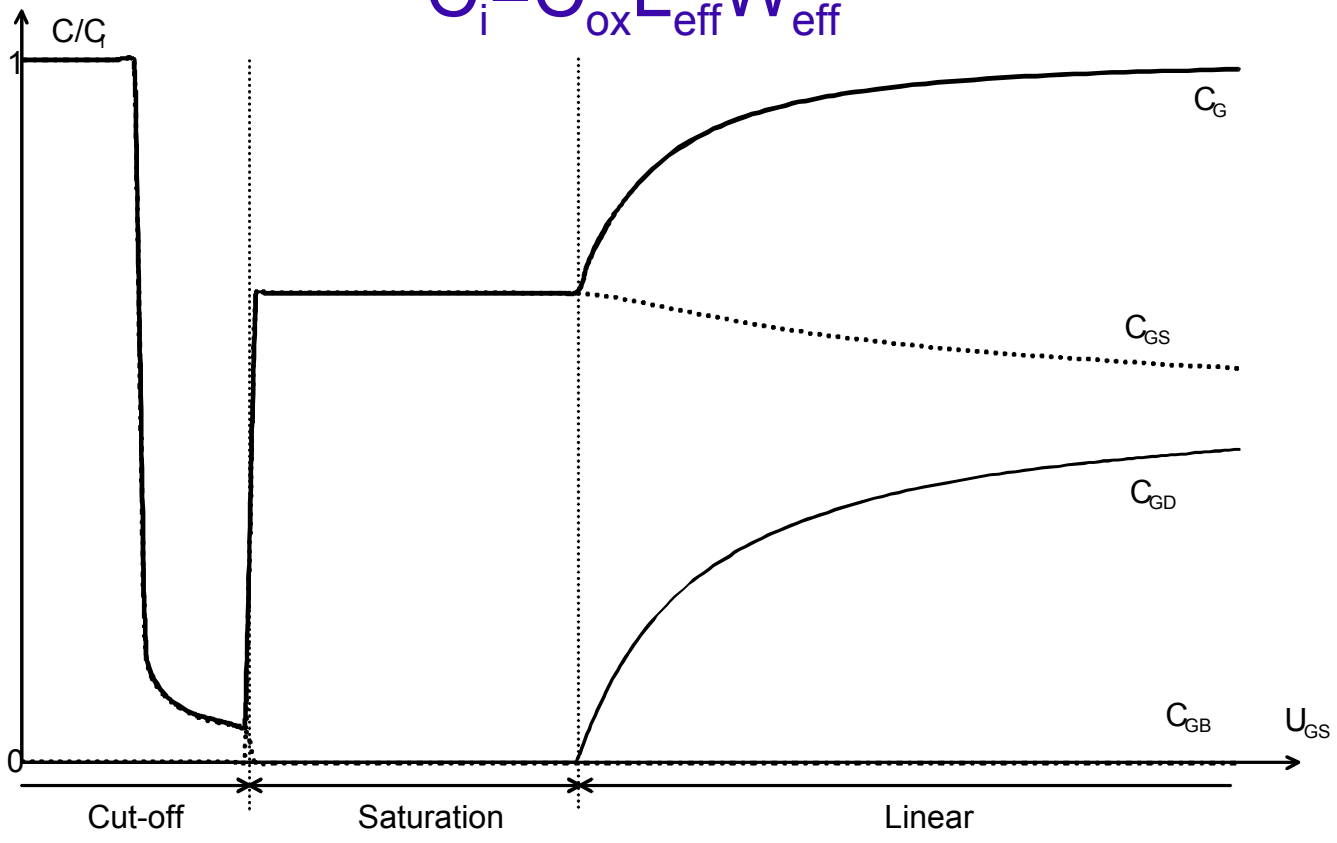
for $U_{GS} \approx U_{GD}$ $C_{GS} \approx C_{GD} \approx \frac{1}{2} C_{ox} W_{eff} L_{eff}$

Saturation range ($C_{GD} = 0$)

$$C_{GS} = \frac{2}{3} C_{ox} W_{eff} L_{eff}$$

Capacitance-Voltage Characteristics

$$C_i = C_{ox} L_{eff} W_{eff}$$



What's Missing in LEVEL3

- Hot carrier effect
- Punch-through
- Non-uniform substrate doping

MOS - Summary

Operation range	**Pin voltages**
Cut-off	$U_{GS}<U_{FB}$
Linear, non-saturation, triode	$U_{GS}\geq V_T$ i $U_{DS}<U_{Dsat}$
Saturation, pentode	$U_{GS}\geq V_T$ i $U_{DS}\geq U_{Dsat}$
Sub-threshold, weak inversion	$U_{FB}\leq U_{GS}<V_T$