



POWER DEVICES AND SYSTEMS LABORATORY

# Exercise 7<sup>A</sup>

## Design and Prototyping of a Switched-Mode Power Converter

Indicatory work plan

Week	Class in the Laboratory	Own Work at Home	Teacher's Office Hours
11–12	Assignment of individual parameters	Board design (Task 1)	Consultation
12–13	Consultation	Power supply design or analysis (Tasks 2 and 3–6 or 7–9)	Consultation Board design approval *
13	Delivery and assembly of pre-defined components	Controller design (Tasks 10–12)	Consultation Electronic design approval *
14	Delivery and assembly of calculated components	Assembly verification ** Transistor selection verification (Tasks 13–16)	
15	Start-up, measurements ** Operation approval	Report completion	Consultation Report approval

\* Ultimate deadline. Solutions must be presented to the teacher beforehand so that there is time available for necessary modifications still before this deadline.

\*\* Tasks described in Manual 7<sup>C</sup>.

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## 1. Printed Prototype Circuit Boards

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### 1.1. Universal Printed Circuit Boards

#### 1.1.a. Board structure

For prototyping the physical circuit, a **universal prototyping printed circuit board** (*universal PCB*) may be used. It is a flat piece of laminate (a plastic made of two different materials), 1 to 2 mm thick, with pre-drilled (frequently at equal distances) **mounting holes** and pre-manufactured (usually one-sided) **solder pads** (the metallisation surrounding the hole, enabling to solder a component's lead or a conductor). Mounting holes are frequently pre-connected with regularly placed metallic **conducting traces**.

As such a board may be used to prototype an arbitrary circuit, it is called 'universal.' Universal PCBs are frequently used for circuit prototyping to avoid the time-consuming PCB design, etching and drilling where it is very likely for the circuit idea still to change multiple times.

Fig. 1 presents a view of an exemplary universal prototype PCB. It is a **single sided** PCB, i.e. with metallic traces manufactured on its one side only (which makes it different from the *double sided* PCBs), where solder pads have been pre-connected. This board has a **lead pitch** of 2.5 mm which means that holes and pads (where component leads may be soldered) are placed at the nodes of a 2.5-millimeter square grid.

Trace layout is similar on most universal PCBs. Multiple short vertical connections are manufactured (the vertical and horizontal directions obviously being conventional). Above and below them, longer horizontal traces are realised that are commonly used to distribute power supply and ground to the particular components. Such traces may also be placed vertically, sparsely distributed in the interior or along board edges (the latter being the case of Fig. 1). A board with such a trace layout is well suited for the present exercise.

A universal PCB may be partitioned into several separate sub-circuits. For example, on the board presented in the photograph, 2 separated sub-circuits can be seen (in its left-hand and right-hand sides). Moreover, each of the sub-circuits has two separate connection rows along two horizontal double middle lines (in the upper and lower board quarter). For these rows, only the long vertical trace along the board edge is common.

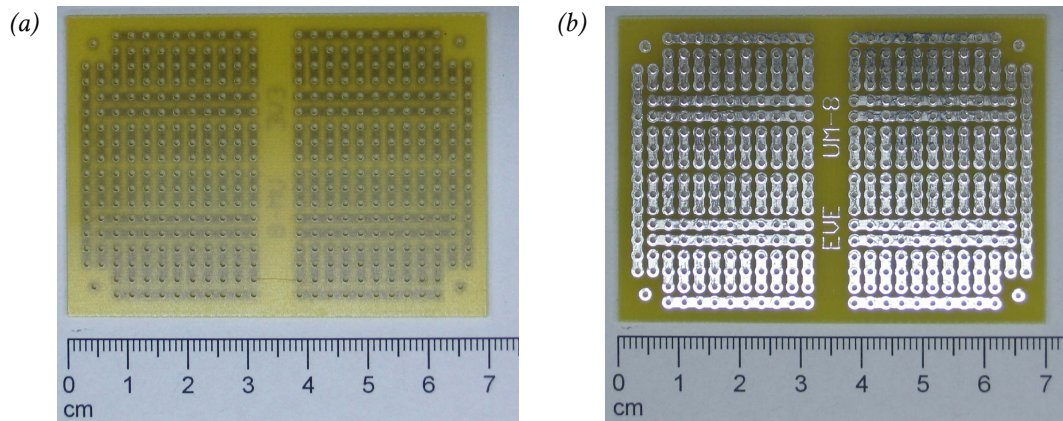


Fig. 1. Single sided universal PCB with pre-connected solder pads  
(a) component side; (b) solder side

As already mentioned, a PCB that has metallisation realised only on its one side is called a single sided PCB. The side on which connections have been manufactured is called the **solder side** whereas the other is the **component side**. Components are essentially placed on the component side (although this is not always the case, especially when a component has to be added). Soldering is done on the solder side.

In the present exercise, the circuit will be realised using the **through-hole technique** (or **through-hole mount**). This term means that component leads are passed through mounting holes to the solder side where they are soldered to solder pads. This technique is very well suited for circuit prototyping because of high soldering speed and the lack of high precision and special care requirements.

However, in final product manufacturing, the **surface-mount technique** (SMT) became more widespread. Sometimes it is necessary or easier to use **surface-mount devices** (components in SMT-dedicated casings, SMD) already at the prototyping stage. For this purpose, special universal PCBs are manufactured that enable soldering an SMD and providing one or more mounting holes per each of its pins. Using these holes and the through-hole technique, a complete circuit prototype can be assembled. Such boards usually do not have metal traces except for those connecting device pins with corresponding mounting holes.

### 1.1.b. Circuit design

As the universal PCB used in this exercise has a pre-manufactured trace layout, circuit design activities are limited to:

- 1) planning the device placement,
- 2) determining if and where additional connections are needed.

Action 2 is usually necessary as a universal PCB obviously is 'universal' only to some extent. Before starting the PCB design. The additional connections are realised in one of the following ways:

- 1) with an ordinary insulated conductor—usually on the component side; both connector ends are passed through mounting holes and soldered to the solder pads just as device leads are;
- 2) with a bare wire, e.g. dedicated silvered copper wire or simply a component lead fragment cut off—usually on the device side (if on the solder side, it is necessary to ensure that the wire does not cause unwanted shorts along its length, also when incidentally deformed); wire mounting is done as previously;
- 3) with solder on the solder side (only possible when neighbouring traces are to be connected)—in this case solder pads are usually not occupied;
- 4) with a longer lead of an element connected to the same voltage as the points being connected (only possible if such a lead exists), bent on the solder side in line with the designed connection— this is a more reliable and easier alternative



to technique 3 as the laminate is often covered with a solder resist layer counteracting solder connecting neighbouring pads.

During universal PCB design the following rules are usually applied.

1. The design process is started with integrated circuit sockets. They are placed in dedicated areas, e.g. in the case of the board shown in Fig. 1 pins would be placed apart at both sides of the double horizontal traces. On larger boards, integrated circuits are usually placed in the middle.
2. Integrated circuits impose particular long traces to be chosen as supply and ground. Usually, supply and ground pins are top left and top right, or top left and bottom left, or top left and bottom right ones—this must be checked in the data sheet. It is desirable that a maximum number of devices are directly connected to a supply (or ground) trace.
3. If the PCB has special solder pads for specific connectors, placement begins with these connectors and then integrated circuits connected to them are placed.
4. After the integrated circuits, other devices are placed. One should start with those devices that are closest (in the electrical schematic or according to functional requirements) to the integrated circuits. De-coupling capacitors are placed first.
5. When placing passive elements, the designer should take advantage of the possibility of shorting or—the opposite—leaving long device leads. Vertical mount and appropriate shorting of the leads of an axial case enables inserting them even in neighbouring holes. On the other hand, making use of their full (or slightly shortened) length may eliminate the need for additional connections.
6. It should be kept in mind that device cases have determinate geometrical dimensions. They may cover up and make inaccessible some neighbouring mounting holes. This especially concerns electrolytic capacitors, coils, larger diodes and transistors, diode bridges, buttons, potentiometers and connectors.
7. Device terminals that are mutually connected in the electrical schematic should be placed on one conducting trace. Only when this is impossible, an additional connection is made.
8. Two solder pads should be provided for each additional connection. When neighbouring traces are to be connected, this may be done using solder itself (and possibly an additional supporting wire) on the solder side, without occupying any mounting holes, as described above.
9. No loops should be created together with the additional connections, i.e. moving along traces and additional connections in a chosen direction, we should never get back to the starting point. Loops will behave as antennas, emitting and intercepting electro-magnetic disturbances which may cause improper circuit operation.
10. If coils are present in the circuit (not the case of the present exercise), it should be avoided to place them in the vicinity of integrated circuits or above traces connected to any other devices.
11. Power loops (high-voltage or high-current ones) should have the shortest perimeter and the lowest area enclosed possible. Their elements should therefore be placed the closest possible one to another.
12. Additional connections in high-current loops are realised using high-cross-section wires. Due to the low diameter of mounting holes, it may be necessary to solder these wires on the solder side.
13. Also the leads of high-current devices may have a diameter larger than the diameter of mounting holes. This should be checked on the board design stage (in device data sheets) or after devices are collected (empirically) but *before* circuit assembly starts. Too tight holes will have to be broadened using a drill, taking special care not to damage the solder pads and adjacent traces.

14. Device placement is usually finalised with connectors and potentiometers, which must be put in easily accessible points. These frequently are the board edges. Connection paths to the rest of the circuit should be the shortest possible and should involve the least possible number of additional connections.
15. In the case of prototypes, additional horizontal shorts, vertical measurement pins or measurement points (small loops) are mounted on the board. There are intended to enable attaching oscilloscope probes to the key circuit nodes during testing.

## 1.2. Using the worksheet and design example

### 1.2.a. Design support worksheet

In order to limit the number of errors and to ease design verification, you should use the worksheet *plytka\_uniwersalna.ods* if designing with the prototype board. A general description of this worksheet is available as an attachment to this manual.

Now we will follow an exemplary design based on a universal PCB. Let's assume that the circuit shown in Fig. 2 has to be assembled and that the universal prototyping board already presented in Fig. 1 is to be used.

### 1.2.b. Circuit for the design example

The exemplary circuit has a supply input through the Z<sub>1</sub> connector (a terminal block) and a double signal input through the Z<sub>2</sub> connector. The supply is stabilised with the C<sub>1</sub> electrolytic capacitor. High-frequency disturbances are carried off to the ground through the C<sub>2</sub> de-coupling ceramic capacitor.

The U<sub>1</sub> integrated circuit includes 4 NAND gates numbered from 1 to 4 whose inputs are labelled as A and B, and outputs as Y. The VCC pin is the supply positive potential and the GND pin is the supply ground. These gates are used as buffers for signals 1 and 2 that come from some outputs with too low a current capability to make the Light Emitting Diodes (LEDs) light up. In the case of the signal 1 it is an inverting buffer as a single NAND gate with shorted inputs acts as a NOT gate. For the signal 2 it is a non-inverting buffer as two such NOT gates are connected in cascade.

Gate outputs are supplied from a voltage connected to the VCC and GND pins, so from the source connected to the circuit through the Z<sub>1</sub> connector. We assume that current capability of this source is sufficient to light up the LEDs. Setting a given Y output in the logical zero state, i.e. the low level, means electrically connecting this output to the GND pin, so the ground. In the case of 1Y and 4Y outputs this will close a loop starting from Z<sub>1</sub> connector's terminal 1 and ending at its terminal 2: through D<sub>1</sub> and R<sub>1</sub> or through D<sub>2</sub> and R<sub>2</sub> components. This will enable current flow and lighting up the corresponding LED.

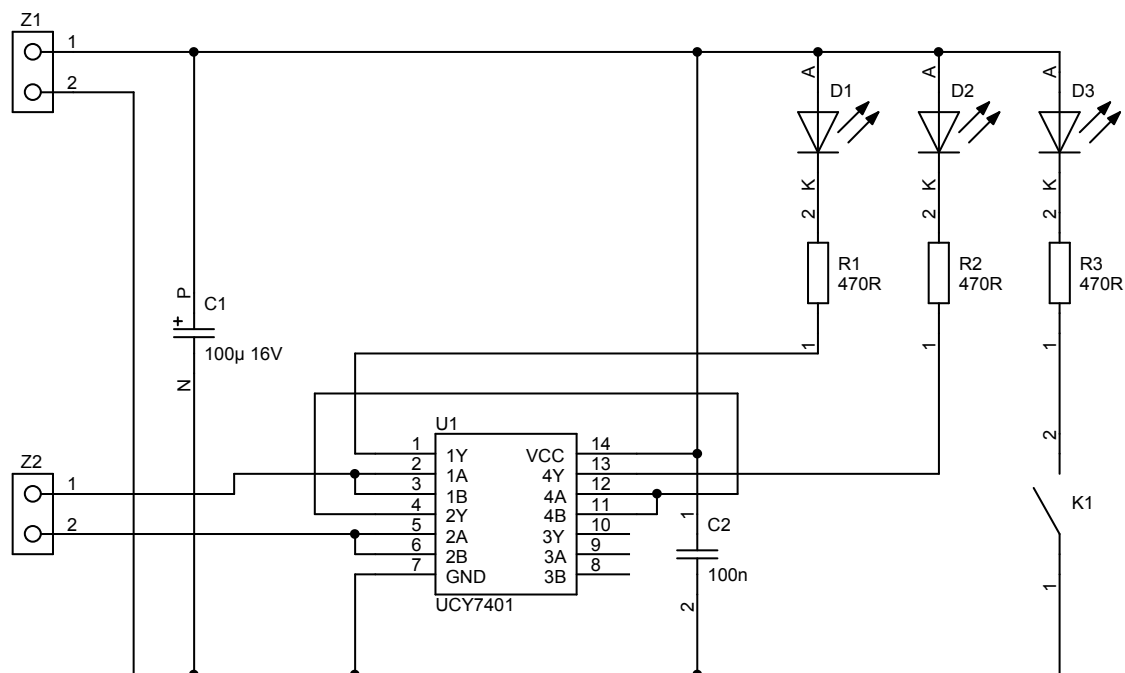


Fig. 2. Schematic of the circuit used in the design example

The third LED (D<sub>3</sub>) is supplied directly and turns on when the K<sub>1</sub> button is pushed (or the key is closed). The 3 resistors R<sub>1</sub>, R<sub>2</sub> and R<sub>3</sub> enable setting the diode current value, which is equal to the supply voltage decreased by the voltage drop across the diode and divided by the resistor's value.

**1.2.c. Preparation for design**

In order to start the design, it is necessary to know the lead arrangement and spacing for the particular components as well as their case dimensions (precisely, the dimensions of case projection onto the board surface). Together with professional PCB design software, case outline libraries are delivered. In our case, outlines and lead arrangement are shown in Table 1 against the solder pads grid of the board to be used (so, a single distance between holes is 2.5 mm).

The universal board together with all the components are pictured in Fig. 3.

Table 1. Lead arrangement and case outline for the components used in the design example (terminal labels are consistent with Fig. 2)

Component	Integrated circuit, DIP-14	Miniature button
Case outline with lead arrangement		
Component	Terminal block, 2-pole, RM 5	Electrolytic capacitor, vertical, Ø6, RM 2,5
Case outline with lead arrangement		
Component	Light Emitting Diode	Capacitor, ceramic disc
Case outline with lead arrangement		
Component	Resistor, 1/4 W, horizontal mount	Resistor, 1/4 W, vertical mount
Case outline with lead arrangement		

Design begins with the entry of the solder pads and connecting traces image to the spreadsheet *Płytką*, the effect being presented in Fig. 4. Grey represents the laminate surface, white represents metallic paths (traces) and black frames represent solder pads (so, mounting holes as well).

Into the spreadsheet *Węzły schematu* data about electrical connections in the circuit according to Fig. 2 are introduced. The considered circuit has 11 electrical nodes which results in the below circuit description.

- Z1.1 C1.P U1.14 C2.1 D1.A D2.A D3.A
- Z1.2 C1.N U1.7 C2.2 K1.1
- Z2.1 U1.2 U1.3
- Z2.2 U1.5 U1.6
- U1.4 U1.11 U1.12
- U1.1 R1.1

R1.2 D1.K  
 U1.13 R2.1  
 R2.2 D2.K  
 K1.2 R3.1  
 R3.2 D3.K

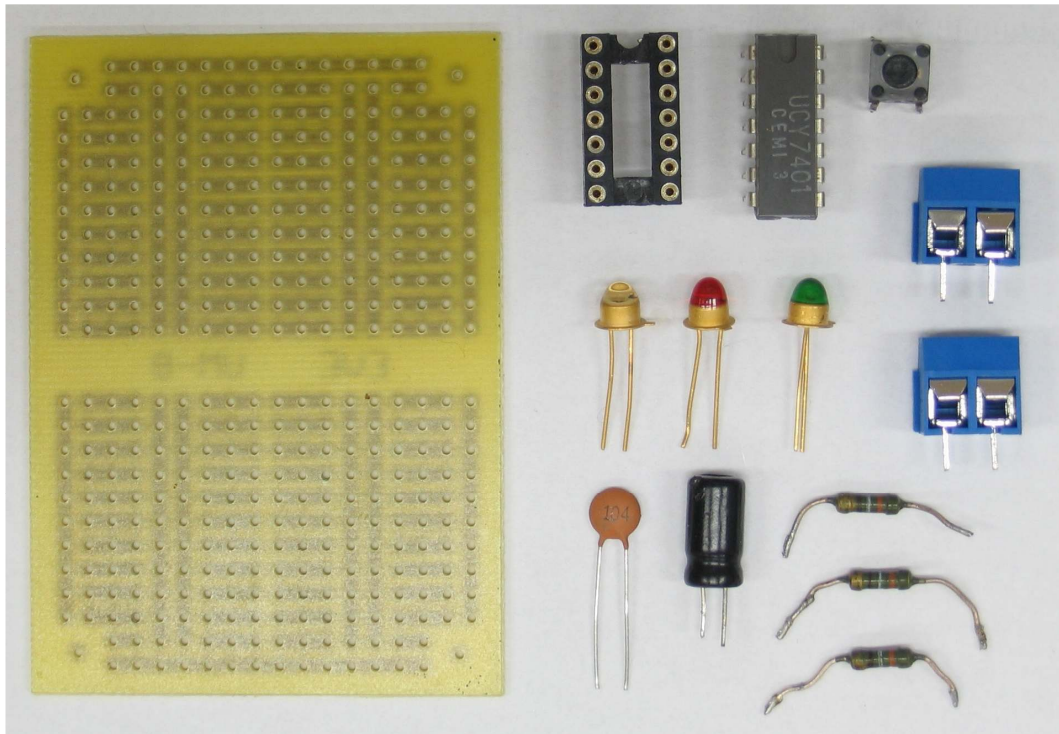


Fig. 3. Board and components for the design example

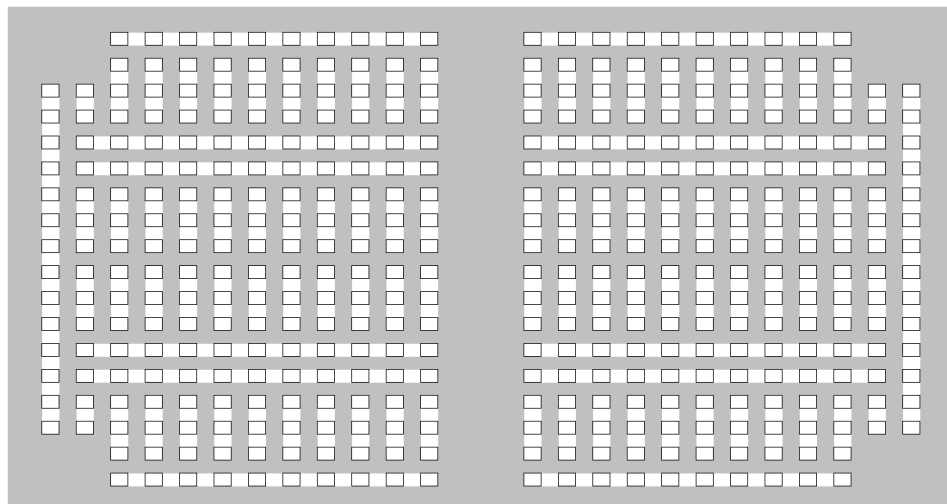


Fig. 4. Solder pads and pre-manufactured connections image defined in the spreadsheet *Płytki*

#### 1.2.d. Component placement and connection planning

We are now beginning the design process proper.

1. We start with the  $U_1$  integrated circuit (see Section 1.1.b, pt 1. We will place it along one of the long horizontal traces. As it has two input signals connected from the left-hand side (in the schematic) and the  $Z_1$  terminal block has fairly large dimensions, we decide to locate the IC in the bottom left quarter of the board, so that there is enough space for the terminal block above it (on the board). On the other hand, right of the IC (on the board) we leave free space for the  $C_2$  de-coupling capacitor. The result is shown in Fig. 5(a).

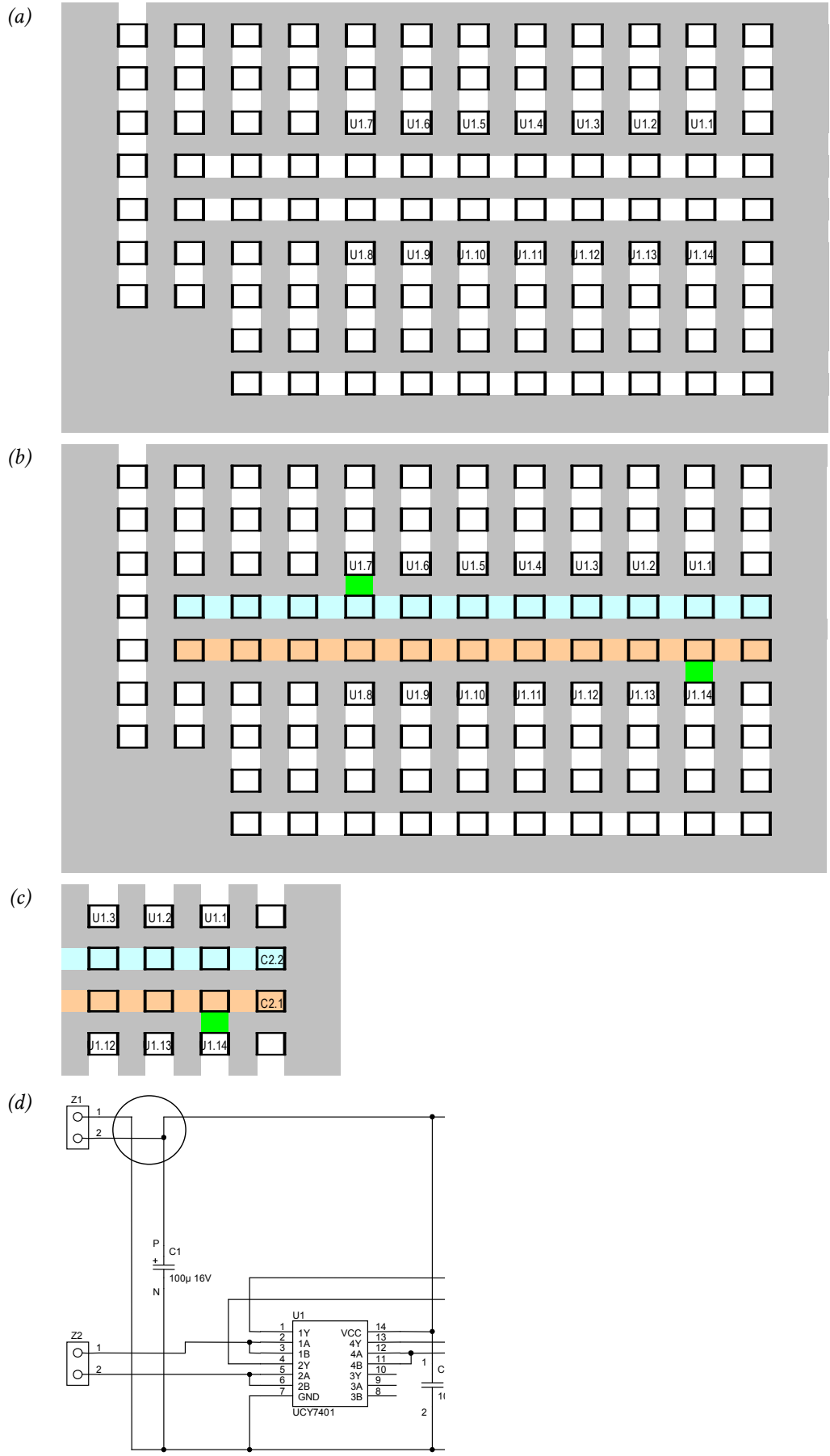


Fig. 5. Board design process

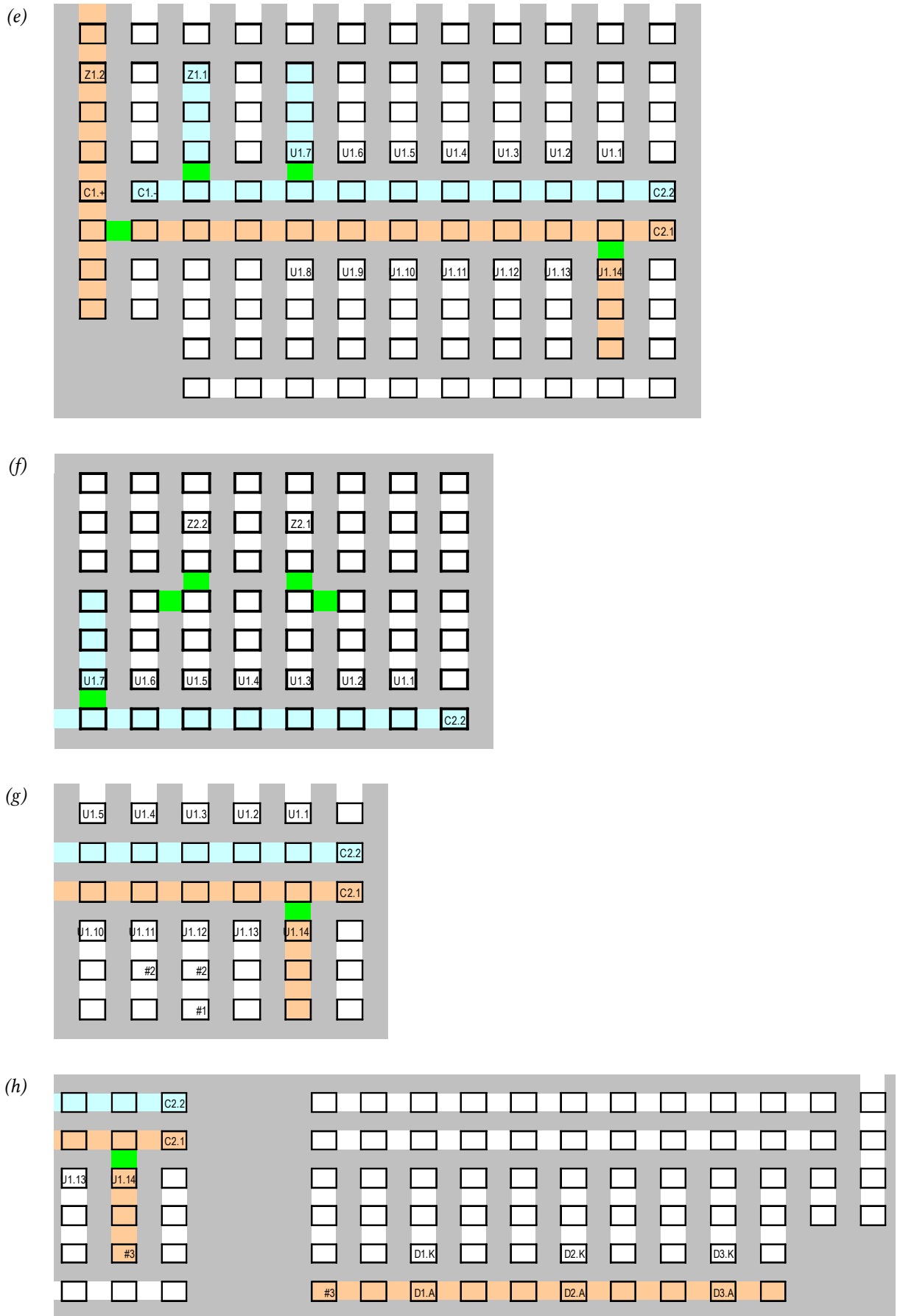


Fig. 5 (cont.) Board design process

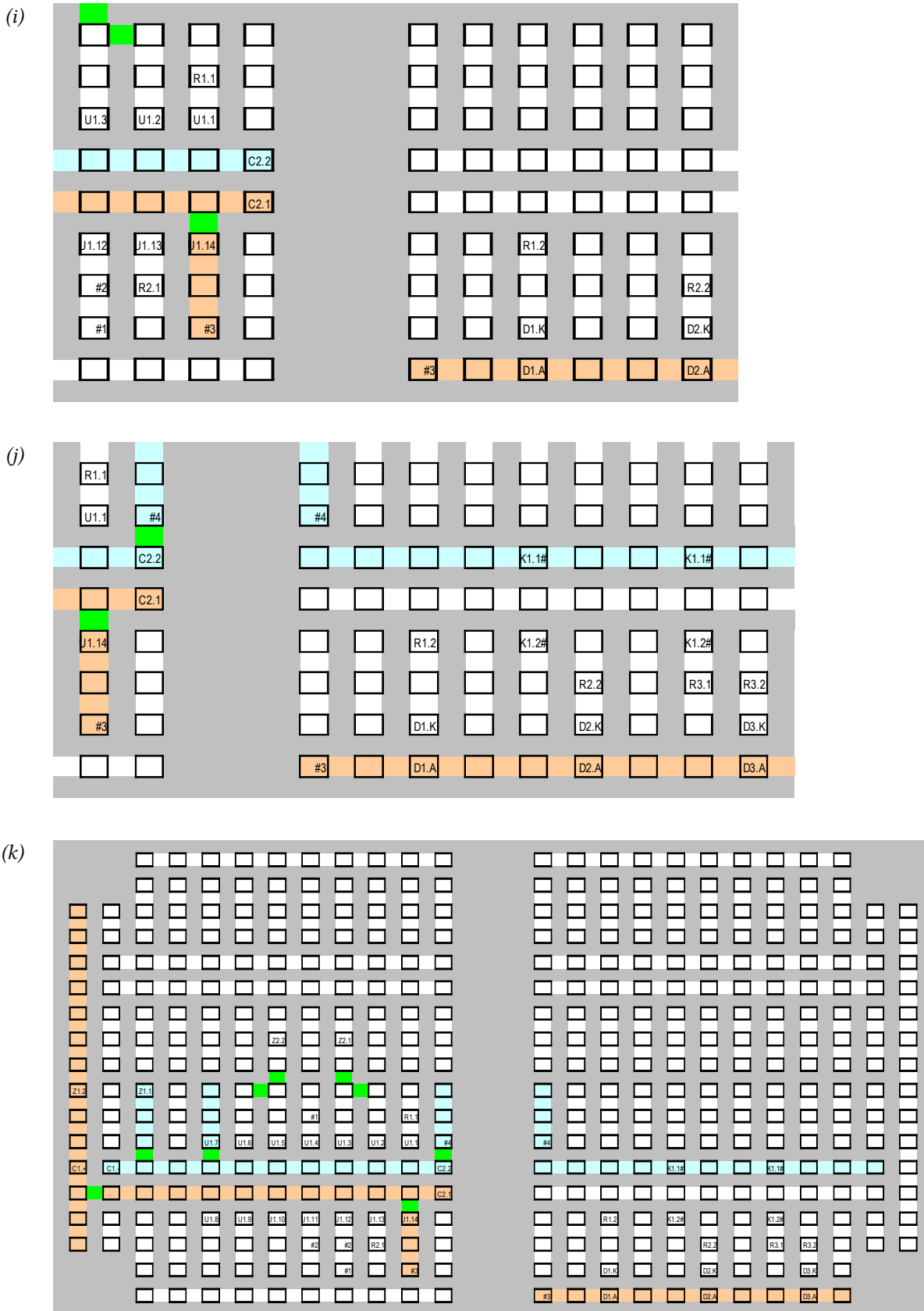


Fig. 5 (cont.) Board design process

2. The IC imposes specific long horizontal traces to be chosen as supply (the one neighbouring the pin 14 or VCC, see Section 1.1.b, pt 2) and as ground (the one neighbouring the pin 7 or GND). We mark them with pink and cyan and connect to the appropriate pins of the U<sub>1</sub> integrated



circuit using solder on the solder side (a wire can be avoided as neighbouring traces are being connected, see Section 1.1.b, pt 8), which we mark with green. The result is shown in Fig. 5(b).

3. The  $C_2$  de-coupling capacitor is inserted between the supply and ground traces, the closest possible to the supply pin (VCC) of the  $U_1$  IC (see Section 1.1.b, pt 4), taking care to connect terminal 2 to the ground and terminal 1 to the supply. Otherwise, the automated design check will fail because the board will be incompatible with the schematic. The result is presented in Fig. 5(c).
4. On the left end of the supply traces there is enough space for connecting the supply (the  $Z_1$  terminal block) and the  $C_1$  blocking capacitor. It is best to insert the capacitor directly into the traces as there will so be no need for any additional connections; in this case, we will place the terminal block above the capacitor. The supply path has therefore to be bent to the top (towards the terminal block), for which purpose we use the long vertical trace along the board's edge. The ground trace will be bent along the shorter path. We plan to make all the necessary connections using solder on the solder side. We update supply and ground path colouring and check whether they do not form a loop (see Section 1.1.b, pt 9).

If the terminal block was to be inserted according to the schematic, i.e. with the ground connected to  $Z1.2$ , the front of this block would have to face the  $C_1$  capacitor, which would impede inserting wires (see Section 1.1.b, pt 14). We therefore insert it with its *back* facing the capacitor which forces us to modify the electrical schematic by connecting the ground to  $Z1.1$  and the supply to  $Z1.2$  [see Fig. 5(d) where a circle shows the modified part]. The final result is presented in Fig. 5(e).

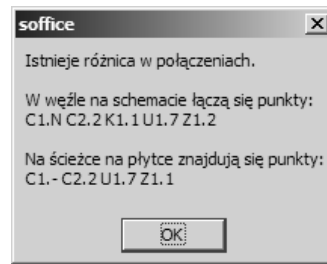
5. Now we can place the  $Z_2$  terminal block, however, making sure to leave enough space between it and the IC to make the connections going out from pins 1 and 4. We can notice that it will be profitable to locate the  $Z2.1$  pin just opposite the  $U1.3$  pin, and  $Z2.2$  opposite  $U1.5$  because such connections are present in the electrical schematic. We short the pins as appropriate,  $U1.2$  with  $U1.3$  and  $U1.5$  with  $U1.6$ , using solder as they are placed on neighbouring traces. The result is presented in Fig. 5(f).
6. We make last connections in the vicinity of the IC:  $U1.4$  with  $U1.12$  using a wire that we label #1 and  $U1.12$  with  $U1.11$  using a wire that we label #2. The result is presented in Fig. 5(g).
7. Only diodes and resistors are left for placement now (except for the  $K_1$  button that we will keep aside until the location of  $R_3$  and  $D_3$  components connected with it is determined). As all the three anodes must be at the supply potential, we will connect them to one of the long traces (see Section 1.1.b, pt 7). We choose the one running along the edge of the bottom right quarter of the board because it is located relatively close to the IC and there is enough space above it for the three resistors and the button. The supply is brought to this trace from pin 14 of the IC using the wire #3. We should keep in mind that according to the table, each diode occupies about 3 solder pad distances (see Section 1.1.b, pt 6). The result is presented in Fig. 5(h).
8. The leads of  $R_1$  and  $R_2$  resistors are originally longer than the minimum lengths shown in Table 1. We can take advantage of this to make direct connections between the cathodes of  $D_1$  and  $D_2$  and the corresponding outputs of the IC, without using any additional wires (see Section 1.1.b, pt 5). We must only try to avoid their crossing with other components or provide an appropriate (vertical) distance between them, or protect the leads with insulating tubes. The result is presented in Fig. 5(i).
9. On the contrary, the  $R_3$  resistor will be mounted vertically, to fit the  $K_1$  button just beside. The button will be placed in such a way that its other end is inserted into the long horizontal line. We continue along this line to the left, to a point nearest the existing ground trace, and we insert the wire #4 for the missing part of the connection. Due to the closest solder pad being occupied by the  $C2.2$  terminal, we insert the other end of the wire do the neighbouring, free pad and connect to the ground trace using the solder.

Attention should be paid to terminate the labels of the  $K_1$  button's terminals with the hash sign “#” as they are shorted in pairs inside the component. In order for this to be taken into account during design check, both terminals of a pair must be given the same label which moreover must end with a hash sign (see the worksheet description attached).

10. Component placement is finished. The result is presented in Fig. 5(k).

### 1.2.e. Design verification and improvement

11. We will now check the correctness of our design using the macro *\_SprawdzPolaczenia*. Verification causes an error message to be displayed telling us about discrepancy in connections between the schematic and the board:



In the 3<sup>rd</sup> line of such a message, terminals connected to a same node in the schematic are listed. In the 5<sup>th</sup> line, terminals connected to the same node on the board are listed. We can state that there are 3 differences between these lists:

- 1) there is a C1.- terminal on the board which, according to the schematic, should be labelled C1.N; on this occasion, C1.+ should obviously be also changed to C1.P;
- 2) the K1.1 terminal is not present in the board-based list which means we have not connected it to the ground; indeed, we have mistakenly placed the second end of the wire #4, opposite the first one instead of one solder pad below; we move it to the proper location;
- 3) the trace corresponding to the displayed list connects to Z1.1 while based on the schematic it appears that it should connect to Z1.2; in this case, this is the sheet *Węzły schematu* that is wrong as we forgot to update it after the connections of the Z<sub>1</sub> connector were exchanged.

After correcting, the schematic is described as follows:

```
Z1.1 C1.N U1.7 C2.2 K1.1
Z1.2 C1.P U1.14 C2.1 D1.A D2.A D3.A
Z2.1 U1.2 U1.3
Z2.2 U1.5 U1.6
U1.4 U1.11 U1.12
U1.1 R1.1
R1.2 D1.K
U1.13 R2.1
R2.2 D2.K
K1.2 R3.1
R3.2 D3.K
```

while the new image of the board is presented in Fig. 7.

12. We launch the check again. This time the error concerns the following terminals:

```
Schemat: U1.11 U1.12 U1.4
Płytką:  U1.10
```

where *Schemat* lists the terminals in the schematic and *Płytką* lists the terminals on the board.

We check the unconnected U1.10 terminal which appears in the board-based list and we state that it indeed should be floating. The same applies to U1.9 and U1.8. Unfortunately, we did not allow for it in the node list. We must therefore introduce three additional nodes to the sheet *Węzły schematu*, with only one terminal assigned to each of them. Sheet contents are now as follows:

```
Z1.1 C1.N U1.7 C2.2 K1.1
Z1.2 C1.P U1.14 C2.1 D1.A D2.A D3.A
Z2.1 U1.2 U1.3
Z2.2 U1.5 U1.6
U1.4 U1.11 U1.12
```

U1.1 R1.1  
R1.2 D1.K  
U1.13 R2.1  
R2.2 D2.K  
K1.2 R3.1  
R3.2 D3.K  
U1.8  
U1.9  
U1.10

13. We launch the check again. There is no error now which means that the connections planned on the board are consistent with those described in the sheet *Wzły schematu* that reflects the electrical schematic.

Fig. 6 shows the circuit assembled according to Fig. 7 and operating. The original circuit may be inspected in the laboratory room as is also the case of an exemplary dimmer as designed in the present exercise.

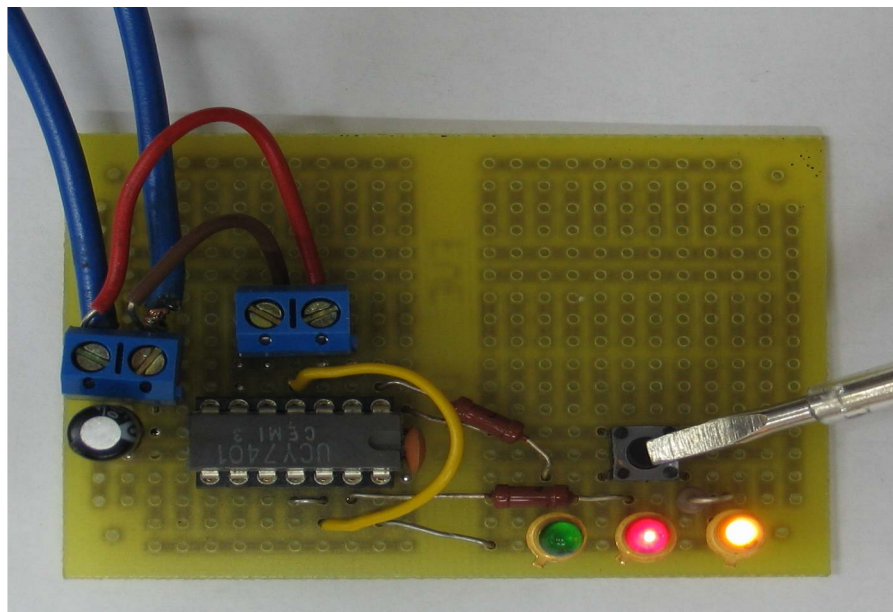


Fig. 6. The example circuit assembled and operating



### 2. Exercise Aim and Plan

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#### What is this exercise for?

#### Circuit realisation on an engineer's work path

The aim of the present exercise is to get acquainted with the most basic issues of prototyping switched mode power electronic circuits. A MOSFET will be used as the controllable semiconductor switch. This exercise is therefore a direct continuation of Exercises 3 and 6, thus filling the gap in the engineer's work path presented in Fig. 8.

During this exercise realisation, you will learn basics of control circuit design for power semiconductor devices based on the principle of variable pulse width. Additionally, you will get acquainted with universal PCB circuit design rules, electronic circuits assembly and the procedures of their starting up and testing.

The present exercise is an occasion to sum up your work of the whole semester. This manual will therefore be referring to knowledge and information from previous exercises. This includes the following problems:

- control of switched mode power electronic circuits through varying the pulse width of the semiconductor switch control signal
  - item 1 (in Fig. 8) ➤ Ex. 3<sup>B</sup>, 4<sup>B</sup>;
- semiconductor device selection considering the requirements imposed by the circuit
  - item 2 ➤ Ex. 1, 5<sup>A</sup>, 5<sup>B</sup>, 6<sup>A</sup>;
- specifics of controlled semiconductor switches operation with real loads
  - item 3 ➤ Ex. 6<sup>B</sup>;
- driving field-effect power semiconductor devices
  - item 3 ➤ Ex. 3<sup>A</sup>, 3<sup>B</sup>;
- static parameters measurement of semiconductor devices
  - item 4 ➤ Ex. 5<sup>A</sup>;
- static parameters measurement of semiconductor devices
  - item 4 ➤ Ex. 3<sup>A</sup>, 4<sup>A</sup>;

- semiconductor device modelling for thermal calculations
  - item 5 ➤ Ex. 6<sup>A</sup>, 6<sup>B</sup>;
- electronic circuit modelling and simulation
  - items 6 and 7 ➤ Ex. 6<sup>A</sup>;
- measurements of voltages, currents and power in electronic circuits using an oscilloscope, a voltage probe, a current probe, a digital multimeter
  - item 10 ➤ Ex. 2, 3, 4, 5<sup>B</sup>, 6<sup>B</sup>;
- work documentation
  - item 11 ➤ all exercises.

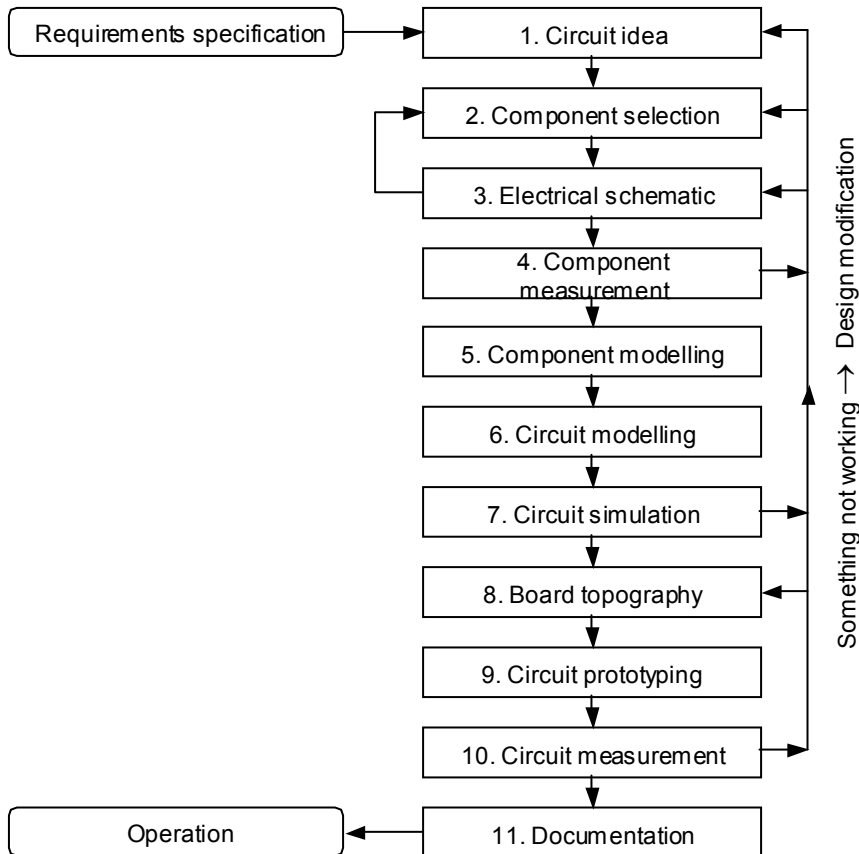


Fig. 8. Work path of a circuit design and prototyping engineer

Exercise 7 will complement the above knowledge and skills in respect of:

- circuit prototype design using a universal PCB: item 8;
- electronic circuit assembly using the through-hole mount technique: item 9.

This manual concerns circuit design, covering items 1 to 8 in the above presented schematic. A next part of the exercise will be devoted to assembly, start-up, operation tests and characteristics measurements (items 9 to 10). The documentation will be created on an ongoing basis.

## What do we aim at?

### Design goals

You should design and prototype a possibly simple dimmer for a halogen lamp desk light with a nominal power of 35 W and a nominal voltage of 12 V, operating in the switched mode and based on the pulse width regulation technique. Some design parameters are set for each team individually. These are included in a table that will be handed over by the teacher.

The original circuit is supplied from the 230 V, 50 Hz mains through a 230 V / 12 V transformer. The dimmer should be inserted between the transformer's secondary winding and the lamp using

wires. Easy connection and disconnection of transformer and lamp-side wires should be ensured. The potentiometer used to adjust light intensity should not be soldered to the PCB directly but connected on wires.

Design parameters have been gathered in Table 2.

Table 2. Design parameters

Dimmer input voltage rms value	$U_{\text{sec}}$	12 V
Dimmer input voltage frequency	$f_{\text{sec}}$	50 Hz
(Rms) nominal voltage of the halogen lamp	$U_{\text{Lh(nom)}}$	12 V
Nominal average power of the halogen lamp	$P_{\text{Lh(nom)}}$	35 W
Dimmer switching frequency	$f_{\text{s}}$	(5...60) kHz *
Minimum duty cycle	$D_{\text{min}}$	0,10...0,20 *
Maximum duty cycle	$D_{\text{max}}$	0,85...0,95 *
Maximum average current drawn by the generator's auxiliary circuit	$I_{\text{R3(av)max}}$	(5...30) mA *
Semiconductor switch	$T_1$	MOSFET *
Rise time for the semiconductor switch	$t_r$	(50...150) ns *

\* Specific data are contained in the attachment handed over by the teacher.

### By what means will we achieve it?

#### Exercise outline

The present exercise may be carried out in one of the following two options:

- (1) **full option** – it comprises the *Supply* and *Control* blocks in Fig. 12 and results in a complete, ready for independent operation, circuit being assembled; there are 22 elements to be arranged and soldered;
- (2) **basic option** – it comprises the *Control* block in Fig. 12 only and therefore the assembled circuit will need an additional *Supply* block, which is available in the laboratory; there are 15 elements to be arranged and soldered.

Choosing the basic option does not influence exercise evaluation negatively. In principle, the full option is meant for people who already have some experience in assembling electronic circuits and consider that the basic option does not fulfil their ambition, or for people that are motivated to gain new skills (the teachers will provide any help needed).

The exercise is carried out according to the following outline:

1. Board design (device arrangement on a universal prototyping PCB or own PCB design): Chapter 4
2. Electronic design (element values selection in chosen functional blocks) with verification through simulation: Chapter 5
3. Circuit prototyping (may be started as soon as the board design is ready but finished only after electronic design is completed)
4. Setting the circuit working and testing for correct operation: Manual 7<sup>C</sup>
5. Measurements of chosen characteristics of the assembled circuit: Manual 7<sup>C</sup>

Carrying out of this exercise must be documented with a report through manually filling in the form that is attached to this manual.

Specific rules for carrying out this exercise are presented in Chapter 6, p. 85.





## 3. DC Chopper

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### 3.1. Circuit idea

#### 3.1.a. Principle of operation

The schematic of the circuit that has been chosen to obtain the dimmer functionality has been presented in Fig 9. It is called a **DC chopper** which reflects the essence of its operation very well. The input voltage  $u_i$  may be constant but also variable with a low frequency  $f_i$  and a corresponding period  $T_i$ . It still is a DC power converter as long as most of the average power is connected with the DC components of voltage and current.

It follows from the schematic that the input voltage is applied across the receiver (the output voltage  $u_o$  with a same period  $T_o = T_i$ ). However, it is not applied directly but *chopped* as the switch periodically, with a frequency  $f_s$  higher than the possible input frequency  $f_i$ , interrupts the application of the input voltage. Waveforms observed in the circuit of Fig. 9, under the assumption that all its components are ideal and that the load is stationary and resistive (of some equivalent resistance  $R_o$ ) is presented in Fig. 10. When the key is closed,  $u_o = u_i$ , and when it is open,  $u_o = 0$ .

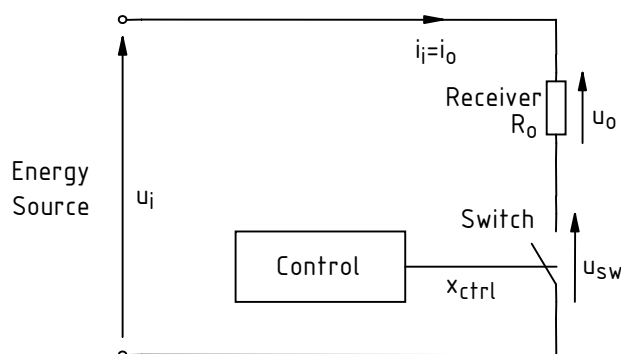


Fig. 9. General schematic of the DC chopper with a resistive receiver

The ratio of the pulse width  $t_p$  of the quantity  $x_{ctrl}$  controlling the switch to the pulse repetition period  $T_p$  is the parameter called the **duty cycle** ➤ Exercises 3<sup>B</sup>, 6. As a result of application of this control signal, the switch is turned on and off with a switching period  $T_s$  (which obviously equals  $T_p$ ). If we assume that the switch is ideal, i.e. switching times are zero, then the switch on-state time  $t_{ons}$  equals the pulse width  $t_p$ . Thus

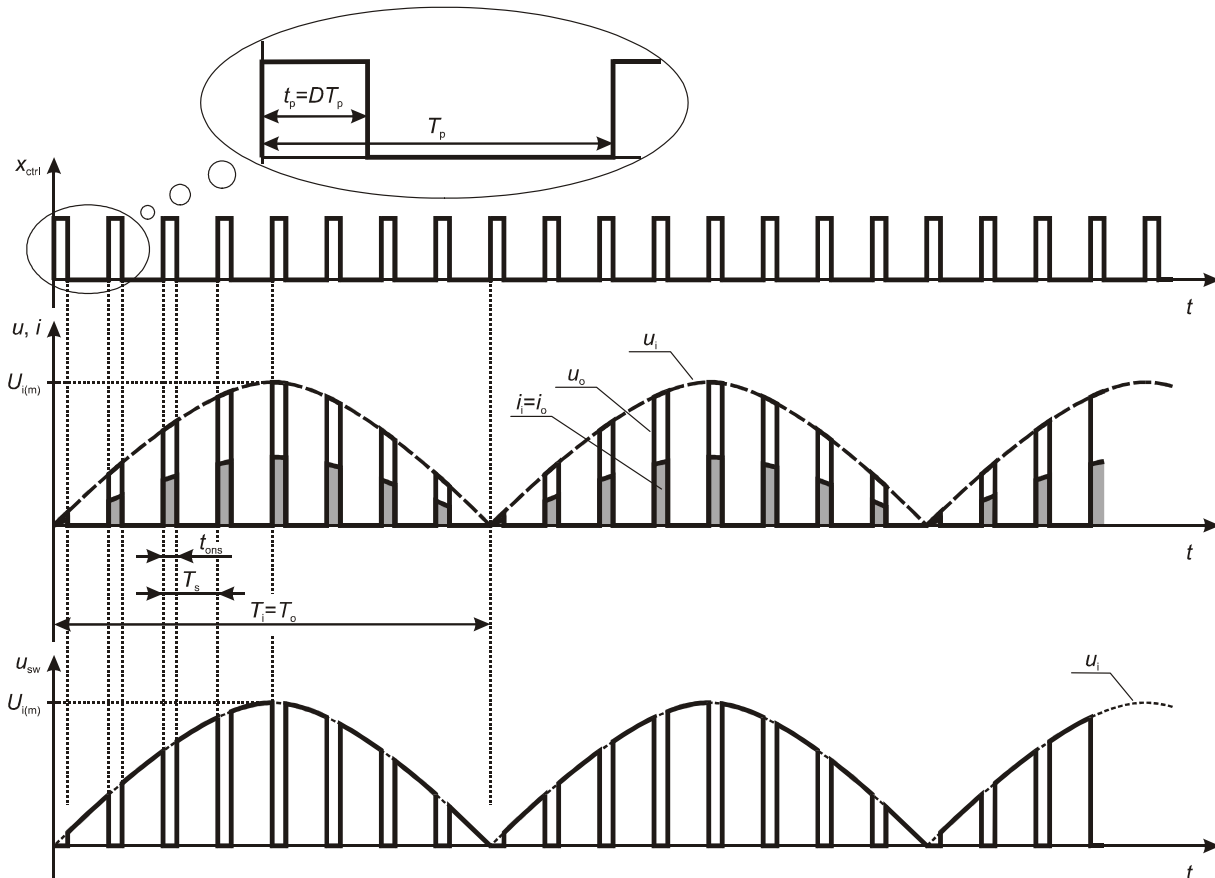


Fig. 10. Current and voltage waveforms in the DC chopper circuit for exemplary input voltage waveform and duty cycle

$$D = \frac{t_p}{T_p} \approx \frac{t_{\text{ons}}}{T_s} \quad (3.1)$$

The operation of the considered circuit is described by two important terms: ➤ Exercises 2, 3<sup>B</sup>

- 1) **switched-mode circuit** which refers to the semiconductor switch being alternately turned on and off with a high frequency (as compared to input waveforms, output waveforms or to various time constants present in this circuit);
- 2) **pulse width modulation** which is the method for obtaining a desired output (current, voltage, power, ...; instantaneous, rms, average, ...) by changing the duty cycle of the pulse waveform controlling the semiconductor switch.

### 3.1.b. Power conversion characteristics

From the rms value definition, the rms output voltage is given by

$$U_{o(\text{rms})} = \sqrt{\frac{1}{T_o} \int_{T_o} u_o^2 dt} \quad (3.2)$$

where  $T_o$  is the  $u_o$  waveform period. It follows from the circuit topology (Fig. 9) and the analysis done in Section 3.1.a that the output voltage period  $T_o$  equals that of the input voltage  $T_i$ . Interrupting the applied to the receiver means making it zero for a given period of time (the switch's off-state duration). Therefore, the rms value of  $u_o$  is lowered when the duty cycle  $D$  is decreased

because the integral decreases ➤ Exercise 2. It may be shown that this is quantitatively described by the formula

$$U_{o(\text{rms})} \approx \sqrt{D} \cdot U_{o(\text{rms})\text{max}} = \sqrt{D} \cdot U_{i(\text{rms})} \quad (3.3)$$

where  $U_{o(\text{rms})\text{max}}$  is the maximum rms output voltage that can be obtained. As can be seen, it is obtained for  $D = 1$ , so without any chopper action, the input voltage being constantly applied to the receiver without any interruption. Therefore, for  $D = 1$ ,  $u_o = u_i$  and

$$U_{o(\text{rms})\text{max}} = U_{o(\text{rms})} \Big|_{D=1} = U_{i(\text{rms})} \quad (3.4)$$

which is already reflected in Eq. (3.3).

For a resistive receiver, the average output power is

$$P_o = \frac{U_{o(\text{rms})}^2}{R_o} \quad (3.5)$$

Substituting (3.3) into the above, we obtain

$$P_o = \frac{U_{o(\text{rms})}^2}{R_o} \approx \frac{DU_{i(\text{rms})}^2}{R_o} = DP_{o,\text{max}} \quad (3.6)$$

where  $P_{o,\text{max}}$  is the maximum average output power, which is obtained for  $D = 1$  and amounts

$$P_{o,\text{max}} = P_o \Big|_{D=1} = \frac{U_{i(\text{rms})}^2}{R_o} = \frac{U_{o(\text{rms})\text{max}}^2}{R_o} \quad (3.7)$$

Taking into account that the load is resistive, we can also derive how the load current varies, based on the Ohm's law:

$$I_{o(\text{rms})} = \frac{U_{o(\text{rms})}}{R_o} = \sqrt{D} \frac{U_{o(\text{rms})\text{max}}}{R_o} = \sqrt{D} \frac{U_{i(\text{rms})}}{R_o} = \sqrt{D} \cdot I_{o(\text{rms})\text{max}} \quad (3.8)$$

where, as can be seen, the maximum rms output current, obtained for  $D = 1$ , is

$$I_{o(\text{rms})\text{max}} = I_{o(\text{rms})} \Big|_{D=1} = \frac{U_{o(\text{rms})\text{max}}}{R_o} = \frac{U_{i(\text{rms})}}{R_o} \quad (3.9)$$

## 3.2. Practical circuit

### 3.2.a. Adaptation to design requirements

The DC chopper has been chosen to solve the technical problem stated in Chapter 2 because of its simplicity. As we will see in this section, it is just a low-side switch, appropriately supplied and controlled ➤ Exercises 3, 4, 6.

The desired function could obviously be realised more efficiently by some more complex circuits (DC choppers, DC converters etc.) On the other hand, there are even less complex solutions such as some AC voltage controllers ➤ Exercise 2. The DC chopper, however, presents several qualities typical for pulse width modulated circuits such as the possibility of obtaining a higher power factor ➤ Exercise 2.

In the present exercise, the DC chopper is supposed to be a dimmer for a 12-volt desk halogen lamp. As the lamp is supplied from the 230-volt network, it has an additional 230-to-12 volt transformer placed in its base, which is reflected in Fig. 11(a). In order to enable inserting the dimmer between the transformer and the lamp, the original circuit has been physically cut in two along the dashed line. A picture of the components that will be used to test the prototyped dimmers is presented in Fig. 11(b).

After inserting the circuit of Fig. 9 in between the appropriate points of the circuit of Fig. 11(a), taking into account the imposed receiver and switch, we obtain a circuit whose block diagram is presented in Fig. 12. The principal waveforms in this circuit are shown in Fig. 13.

### 3.2.b. Practical circuit operation

We will now analyse the operation of the above presented circuit. To ease this analysis, we will neglect any voltage drops across its components. The supply voltage  $u_{\text{sup}}$  with an rms value  $U_{\text{sup}} = 230 \text{ V}$  and a frequency  $f_{\text{sup}} = 50 \text{ Hz}$  is applied to the primary winding of the transformer. The voltage ratio of the transformer  $U_{\text{pri}}:U_{\text{sec}} = 230:12 = 19,2$ , so the secondary-side voltage  $u_{\text{sec}}$  has the rms value  $U_{\text{sec}} = 12 \text{ V}$  and the same frequency  $f_{\text{sec}} = 50 \text{ Hz}$  (see Table 2, p. 23). On its side, the values of the current  $i_{\text{sup}}$  drawn from the mains are 19,2 times lower than those of the secondary current  $i_{\text{sec}}$ .

For the sake of simplicity, we will disregard the dependence of transformer voltage ratio on load (current). Precisely speaking, a nominal voltage ratio given by the manufacturer is only valid for a nominal secondary current. An un-loaded transformer (with secondary winding open) will have a secondary voltage  $U_{\text{sec}}$  higher than it would follow from the nominal voltage ratio; this means that the voltage ratio increases with decreasing load.

It is known that the MOSFET only allows controlled current conduction and voltage blocking in one strictly defined direction: for the current, from drain to source, and for the voltage, with the drain potential higher ➤ Exercises 3, 6. Due to this characteristic, a **full wave rectifier** had to be inserted into the circuit. The most frequently used diode bridge has been used for this purpose ➤ Exercise 5<sup>B</sup>. The result of its operation is a full-wave rectified voltage  $u_{\text{d}}$ , i.e. a waveform with still the same amplitude  $U_{\text{d(m)}} = U_{\text{sec(m)}}$  (still neglecting voltage drops across the diodes) but all the times positive:  $u_{\text{d}} \approx |u_{\text{sec}}|$ .

During each period of the  $u_{\text{sec}}$  voltage, two identical half-sinusoids of the  $u_{\text{d}}$  appear; the frequency of the latter is therefore two times higher. The rectified voltage  $u_{\text{d}}$  is applied between the transistor's source and the upper terminal of the lamp, so it is the input voltage  $u_{\text{i}}$  of the chopper. The frequency of the input voltage is therefore

$$f_{\text{i}} = f_{\text{d}} = 2f_{\text{sec}} = 2f_{\text{sup}} \quad (3.10)$$

The **controller power supply** converts the variable  $u_{\text{d}}$  voltage to a constant one  $U_{\text{CC}}$  needed for the transistor's controller to work. In an ideal circuit, this constant voltage would equal the rectified voltage amplitude  $u_{\text{d(m)}}$ .

The job of the **generator** is to produce a pulse (rectangular) wave  $u_g$  [corresponding to the abstract  $x_{ctrl}$  signal in Fig. 11(a)] with an amplitude equal to  $U_{CC}$  and a high frequency (as compared to the input voltage  $u_i$  frequency  $f_i$ ), used to control the transistor's gate. In order not to complicate the figure, this voltage has been presented as having a frequency  $f_s = 8f_i$ . In reality, this frequency should be considerably higher and does not have to be a multiple of the input frequency. The duty cycle of the  $u_g$  voltage is adjusted manually by the user.

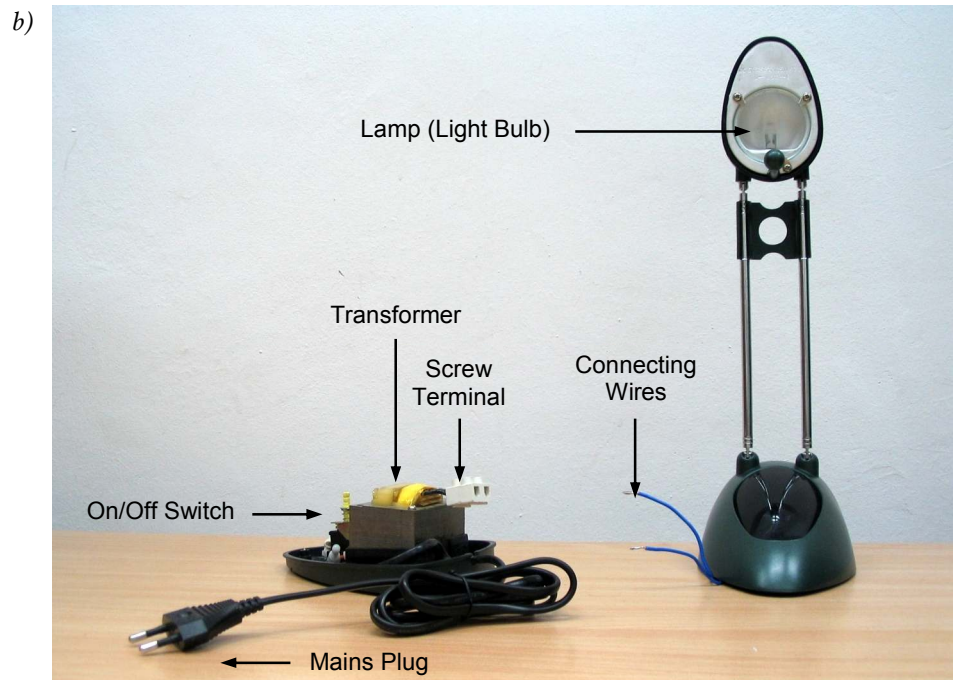
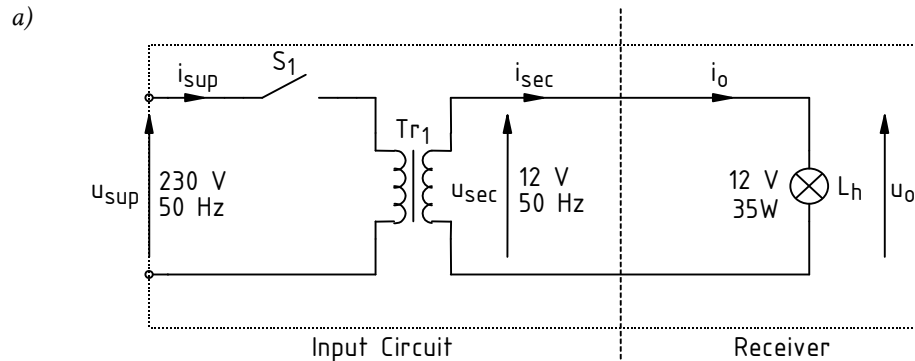


Fig. 11. The initial halogen lamp circuit  
(a) electrical schematic showing the cut line; (b) picture

To make analysis simpler, it has been assumed that the  $u_g$  voltage is identical to the  $u_{GS}$  voltage of the transistor. In reality, these voltages differ due to the action of the transistor's stray capacitances ➤ Exercises 3, 4. However, it can be assumed that their duty cycles are equal (if only transistor switching times are much shorter than the pulse width  $t_p$ ).

Gate-source voltage pulses cause the **transistor** to periodically switch on and off. When the transistor is on, the  $u_d$  voltage is applied across the **lamp** (strictly speaking, reduced by the voltage drop across the transistor). During this period of time, a current flows through the lamp, proportional to  $u_o$  and inversely proportional to the lamp's resistance. The rectifier's input current  $i_{sec}$  is the averaged output current, which results from the filter action of the secondary winding inductance ➤ Exercise 3<sup>B</sup>.

On the other hand, when the transistor is off, the  $i_o$  current is not flowing and the full  $u_d$  voltage appears across this device. The  $u_{DS}$  voltage waveform is obvious (cf. the  $u_{sw}$  waveform in Fig. 10), so it has been omitted in Fig. 13. In a real circuit, overvoltages at the transistor's drain should be expected ➤ Exercise 6<sup>B</sup>. In order to minimise them, a clamping diode has been used. It is therefore

the transistor whose action directly affects the receiver, so this device together with the clamping diode form the **actuator** of the chopper.

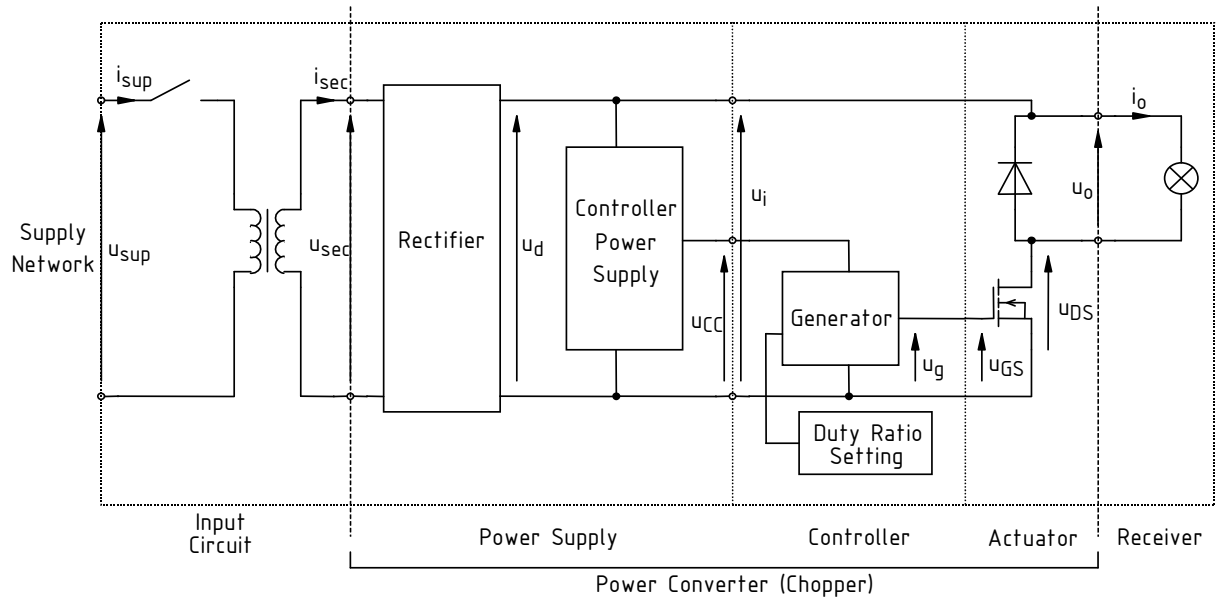


Fig. 12. Block diagram of a complete lamp dimmer circuit based on a DC chopper

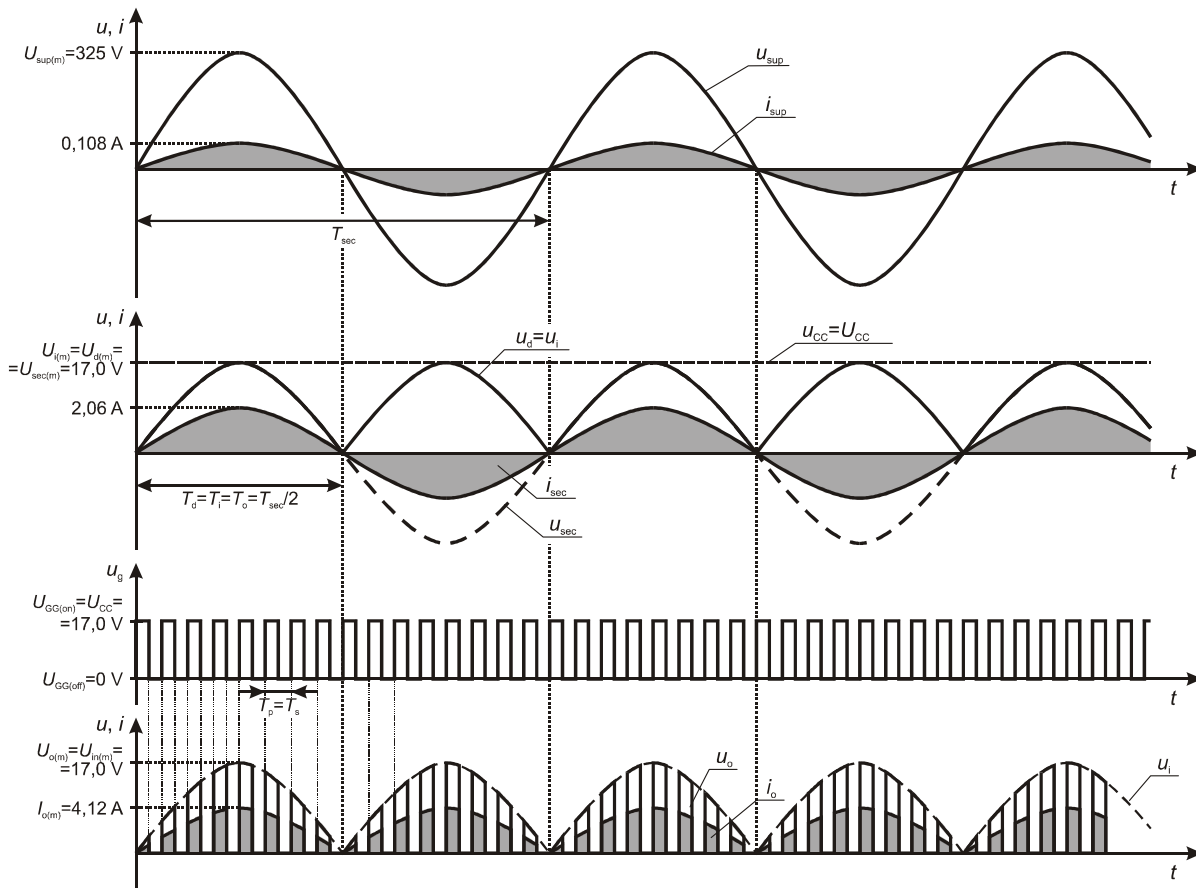


Fig. 13. Simplified waveforms in an ideal DC chopper circuit (Fig. 12)

A duty cyclen of 0,5 has been assumed. Power consumption by the control block, halogen lamp resistance variations and voltage drops across components other than the lamp have been neglected.

### 3.2.c. Detailed schematic and functional blocks

A definitive electrical schematic of the complete circuit with the transformer and the lamp included is presented in Fig. 14. Its part that is the object of design and prototyping has been delimited with dashed lines.

Let us distinguish its functional blocks according to Fig. 12.

1. The **input circuit** (existent) is composed of the circuit breaker (mechanical switch  $S_1$ ) and the transformer  $Tr_1$ . It is supplied with the mains voltage  $u_{sup}$  and a lower voltage  $u_{sec}$  appears on its output.
2. The main constituent part of the **full wave rectifier** is the diode bridge  $B_1$  composed of 4 diodes,  $B_{1A}$  to  $B_{1D}$  (it will be pictured with a simplified symbol in the following schematics). The  $u_{sec}$  voltage coming from the transformer's secondary winding is applied across its AC diagonal (the horizontal one in the schematic) whereas the rectified voltage  $u_d$  appears across the DC diagonal (the vertical one in the schematic) ➤ Exercise 5<sup>B</sup>. On the secondary side, a fuse  $F_1$  has also been inserted in the circuit, which protects the converter against short-circuits.

The large  $C_1$  capacitor serves as a filter whose task is to prevent abrupt variations of the  $u_d$  voltage (see Fig. 12). Such variations would occur at this point of the circuit due to the high-frequency transistor switching. In the moment of transistor turn on, in the circuit formed by the secondary winding, the rectifier and the lamp, an abrupt load change occurs from zero to its maximum value. This would cause an equally abrupt and well apparent drop in the  $u_d$  voltage, resulting from the characteristics of the winding and a voltage drop across the diodes of the bridge. The  $C_1$  capacitor, aided by  $C_2$ , enables keeping  $u_d$  voltage at an almost ideal level, changing only sinusoidally with the  $f_i$  frequency (as in Fig. 13).

3. The **controller power supply** is formed by the  $D_1$ ,  $R_2$  and  $C_3$  components. The large  $C_3$  capacitor stores energy to supply the integrated circuit and the transistor's gate when the  $u_d$  voltage is below  $u_{CC}$ . On the other hand, when  $u_d > u_{CC}$  (precisely,  $u_{CC}$  plus the threshold voltage of the  $D_1$  diode), this capacitor is charged from the output of the diode bridge. The  $D_1$  diode acts as a barrier, enabling only charging the capacitor from the bridge and preventing its discharge in the opposite direction.

At the output, i.e. across the terminals of the  $C_3$  capacitor, a voltage  $u_{CC}$  is obtained, slightly lower than the  $u_{d(m)}$  amplitude, which is a result of the voltage drop across the diode, the capacitor's stray series resistance and its finite capacitance. Under the assumption of ideal filtering, it can be assumed that the  $u_{CC}$  voltage has a constant value which we will denote  $U_{CC}$ .

The controller power supply is actually a simple diode rectifier with a capacitor filter, where  $D_1$  is a typical rectifier diode ➤ Exercise 5<sup>B</sup>. However, this circuit is supplied unconventionally, with a variable positive voltage of a double mains frequency. This affects its operation only in a positive manner as the capacitor is charged more frequently, which enables using a smaller  $C_3$  capacitor.

4. **Pulse wave generator with duty cycle setting** has been based on the  $U_1$  integrated circuit and the  $R_4$  potentiometer.

The NE555 integrated circuit generates a pulse (rectangular) waveform of a given frequency and duty cycle ➤ Exercise 3<sup>B</sup>. Both these values result from the value of the  $C_4$  capacitor and values of components that form the setting circuit: the constant resistances of  $R_3$  and  $R_5$  and the present setting of the  $R_4$  potentiometer. Generator operation will be addressed in more detail in Section 1.1.

The NE555 integrated circuit also serves as the gate driver for the MOSFET, enabling delivery of an appropriate charge in an appropriate time. Remind that

it is not sufficient to apply a voltage between the gate and the source to turn on a power MOSFET. One must also assert an appropriate current flow to charge the input capacitance to the given voltage level ➤ Exercise 3<sup>A</sup>. The NE555 version that will be used, thanks to being based on bipolar transistors, enables delivering and sinking a considerable current.

The control circuit is complemented by the  $R_6$  resistor that sets the transistor's switching times ➤ Exercise 3<sup>A</sup>.

5. The **actuator block**, i.e. where a control signal ( $u_g$  in this case) is converted to some action affecting the receiver (switching the receiver current on and off in this case), is the  $T_1$  MOSFET in the low-side switch topology aided by the overvoltage protection diode  $D_3$  ➤ Exercises 3, 6.
6. The **receiver** (existent) is obviously the 35-watt halogen lamp  $L_h$ .

### 3.2.d. Conditioning and protection devices

Switching the transistor with high speed and frequency causes transitory disturbances to appear that propagate along conducting traces and through parasitic capacitances. They can interfere with the operation of the integrated circuit or of the transistor, e.g. causing its undesired turn-on. In the extreme case, a disturbance can cause a permanent device failure.

Some components of the considered circuit protect it from such undesired effects. They include:

- (1) the  $D_3$  diode which reduces overvoltages resulting from parasitic inductances in the load circuit, thus limiting disturbances and protecting the transistor ➤ Exercise 6<sup>B</sup>;
- (2) the  $R_7$  resistor reduces the gate's sensitivity to the abovementioned disturbances and to electrostatic discharge (ESD) as well, enabling any extra charge to be carried out to the ground instead of charging the gate-source capacitance;
- (3) the  $C_5$  capacitor, called the **de-coupling capacitor**, protects the integrated circuit from negative consequences of overvoltages and undervoltages occurring in its supply;
- (4) similarly, the  $C_6$  capacitor protects an internal reference voltage of the integrated circuit;
- (5) the  $C_2$  capacitor helps the  $C_1$  capacitor filter the  $u_d$  voltage in the high frequency range and prevents any high-frequency disturbances to get through back to the supply network.



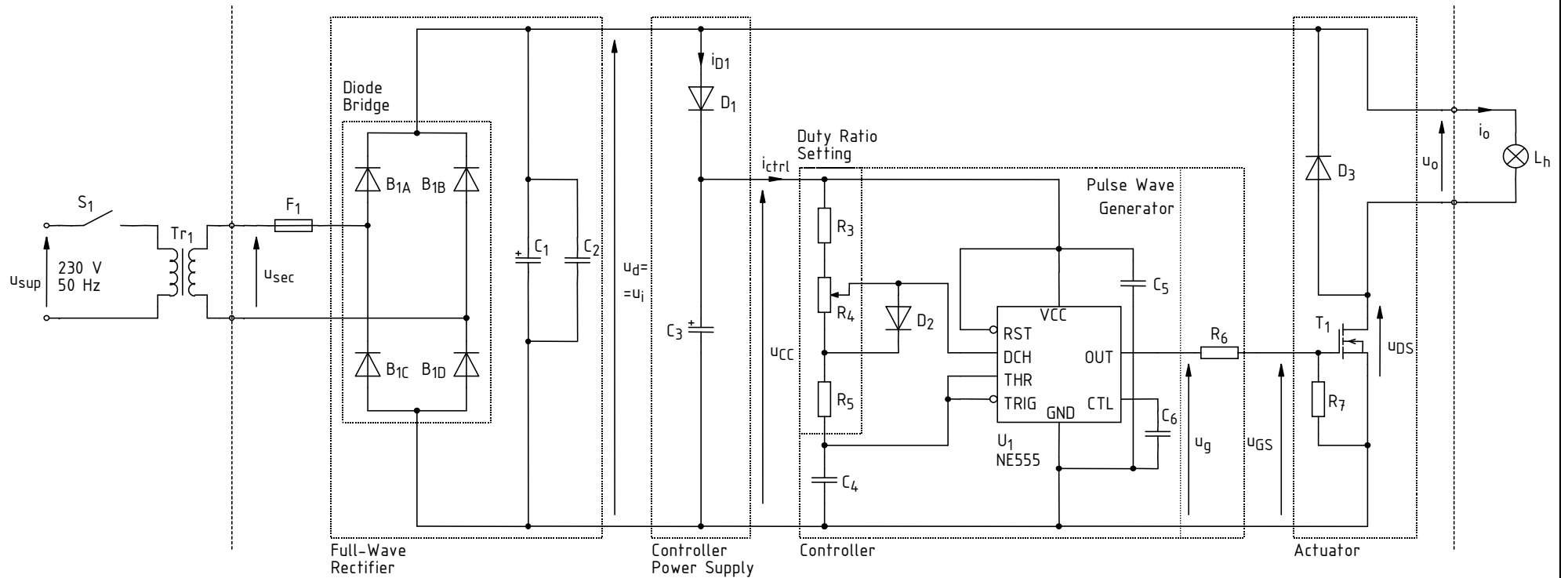


Fig. 14. Complete electrical schematic of the system with the dimmer (dashed lines mark off parts that exist and those to be assembled)

### 3.3. Pulse wave generator

#### 3.3.a. Basic astable configuration

In order to design the controller, it is necessary to understand the operation of the 555 timer. Its basic operating principle has been described in Ref. [19], “Monostable Operation” and “Astable Operation” Sections. In this data sheet, formulae have been derived for the charge  $t_{\text{ch}}$  and discharge  $t_{\text{dch}}$  times in the case of astable operation:

$$t_{\text{dch}} = 0,693\tau_{\text{dch}} = 0,693R_2C \quad (3.11)$$

$$t_{\text{ch}} = 0,693\tau_{\text{ch}} = 0,693(R_1 + R_2)C \quad (3.12)$$

where  $\tau_{\text{ch}}$  and  $\tau_{\text{dch}}$  are the exponential charge and discharge time constants. These formulae, together with general relationships for pulse (or switching in the future) frequency  $f_p$  and duty cycle  $D$ ,

$$f_p = \frac{1}{T_p} = \frac{1}{t_{\text{ch}} + t_{\text{dch}}} \quad (3.13)$$

$$D = \frac{t_{\text{ch}}}{T_p} = \frac{t_{\text{ch}}}{t_{\text{ch}} + t_{\text{dch}}} \quad (3.14)$$

enabled deriving the final relationships that can be used in design:

$$f_p = \frac{1}{0,693(R_1 + 2R_2)C} \quad (3.15)$$

$$D = \frac{R_1 + R_2}{R_1 + 2R_2} \quad (3.16)$$

It is self-evident to change the  $D$  ratio using a potentiometer, such as  $R_4$  in Fig. 14. In such a case,  $R_1$  and  $R_2$  represent the currently set resistances of the first and second sections of the potentiometer, and their sum is always constant and equals the potentiometer total resistance:

$$R_1 + R_2 = R_p = \text{const} \quad (3.17)$$

which follows from the mechanical design of this component. Let us denote the current potentiometer's division ratio with  $k$ ,

$$k = \frac{R_1}{R_1 + R_2} = \frac{R_1}{R_p} \quad (3.18)$$

Then,

$$D = \frac{2k - 1}{3k - 2} \quad (3.19)$$

$$f_p = \frac{1}{0,693(3k - 2)(R_1 + R_2)C} = \frac{1}{0,693(3k - 2)R_p C} \quad (3.20)$$



- the  $R_1$  resistor corresponds to the total resistance in the path of the charge current, thus of the  $R_3$  resistor, the upper section of the  $R_4$  potentiometer and the  $R_5$  resistor;
- the  $R_2$  resistor corresponds to the total resistance in the path of the discharge current, thus of the lower section of the  $R_4$  potentiometer and the  $R_5$  resistor;
- the  $C$  capacitor is the  $C_4$  capacitor.

The task of the  $R_3$  and  $R_5$  resistors is to limit the duty cycle  $D$  so that the full range of  $[0; 1]$  is not achieved. Operation in regions close to 0 or 1 would cause a hard to predict circuit behaviour. Due to the non-zero switching times of the semiconductor switch, there is some low value of  $D$  for which the transistor stops to switch even though the driving pulse duty cycle is still greater than zero. By analogy, starting from some high value of  $D$ , the transistor will be constantly on even though the driving signal is not yet constant. Operation in some ranges (that cannot be precisely determined now) neighbouring 0 and 1 makes it therefore impossible to vary the lamp light intensity. Additionally, values of  $D$  that are close to the above mentioned boundaries would normally cause an unstable circuit operation: changing light intensity, toggling between on and off, etc.

By applying the symbols of Fig. 14 to the formulae (3.11) and (3.21), we obtain:

$$t_{\text{dch}} = 0,693(R_{4\text{d}} + R_5)C_4 \quad (3.24)$$

$$t_{\text{ch}} = 0,693(R_3 + R_{4\text{g}} + R_5)C_4 \quad (3.25)$$

where the upper section's resistance of the  $R_4$  potentiometer has been denoted as  $R_{4\text{g}}$  and the lower section's one as  $R_{4\text{d}}$ .

Substituting the above to the relationship (3.13), we get the formula for the rectangular waveform frequency in the designed circuit:

$$f_p = \frac{1}{t_{\text{ch}} + t_{\text{dch}}} = \frac{1}{0,693(R_3 + R_{4\text{g}} + R_5)C_4 + 0,693(R_{4\text{d}} + R_5)C_4} \quad (3.26)$$

Considering that the sum of both potentiometer sections' resistances is constant and equals its total resistance  $R_4$ , the above can be simplified to the form of

$$f_p = \frac{1}{0,693(R_3 + R_4 + 2R_5)C_4} \quad (3.27)$$

Next, from (3.14) we obtain

$$D = \frac{t_{\text{ch}}}{t_{\text{ch}} + t_{\text{dch}}} = \frac{0,693(R_3 + R_{4\text{g}} + R_5)C_4}{0,693(R_3 + R_{4\text{g}} + R_5)C_4 + 0,693(R_{4\text{d}} + R_5)C_4} = \frac{R_3 + R_{4\text{g}} + R_5}{R_3 + R_4 + 2R_5} \quad (3.28)$$

The minimum and the maximum duty cycle will be obtained by setting the potentiometer's wiper in either of its extreme positions. For the wiper in its extreme top (according to Fig. 14) position, we have  $R_{4\text{g}} = 0$ , so

$$D_{\text{min}} = \frac{R_3 + R_5}{R_3 + R_4 + 2R_5} \quad (3.29)$$

Whereas for the extreme bottom position,  $R_{4\text{g}} = R_4$ , so

$$D_{\text{max}} = \frac{R_3 + R_4 + R_5}{R_3 + R_4 + 2R_5} \quad (3.30)$$

### 3.3.d. Current consumption

In order to design the generator, we will additionally estimate the required supply current. For the logic part of the integrated circuit, current consumption is given in its data sheet. Still, the auxiliary circuit  $R_1$ – $R_2$ – $C$  together with the discharge transistor must be considered. The current drawn by this circuit is synonymous to the  $R_1$  resistor current  $i_{R_1}$ .

During the capacitor charge phase, current decreases exponentially from a certain initial value down to zero. The initial, maximum current value equals initial voltage across the  $R_1$  resistor divided by its resistance; while it follows from the previous analysis that the voltage across the capacitor is  $\frac{1}{3}U_{CC}$  at that moment. Thus,

$$i_{R_1(\text{ch})}(t=0) = \frac{U_{CC} - \frac{1}{3}U_{CC}}{R_1} = \frac{2}{3} \frac{U_{CC}}{R_1} \quad (3.31)$$

During the discharge phase, current is drawn from the supply only because of the DCH pin being shorted to ground by the transistor which is on. Thus, its value is (after neglecting the voltage drop across the transistor)

$$I_{R_1(\text{dch})} = \frac{U_{CC}}{R_1} \quad (3.32)$$

A maximum average value (over the  $T_p$  period) of the current drawn from the supply will therefore occur when the discharge phase duration is maximum which means  $D = D_{\min}$ ,  $R_1 = R_{1(\min)}$ . To avoid precise calculation of the average value of the current during the charge phase, we will overestimate it by assuming that it is constant. Then,

$$I_{R_1(\text{av})\text{max}} \approx (1 - D_{\min}) \cdot \frac{U_{CC}}{R_{1(\min)}} + D_{\min} \cdot \frac{2}{3} \frac{U_{CC}}{R_{1(\min)}} = \left(1 - \frac{D_{\min}}{3}\right) \cdot \frac{U_{CC}}{R_{1(\min)}} \quad (3.33)$$

where  $R_{1(\min)}$  is the minimum value of the  $R_1$  resistance that can occur in a given application circuit. In the practical circuit of Fig. 14, it occurs when the  $R_4$  potentiometer's wiper is in its extreme top position and equals  $R_3$  because  $R_{4g} = 0$  then.

Under the assumption that  $D_{\min}/3 \ll 1$ , the above formula can be simplified to

$$I_{R_1(\text{av})\text{max}} \approx \frac{U_{CC}}{R_{1(\min)}} \quad (3.34)$$

so using symbols of Fig. 14 it becomes

$$I_{R_3(\text{av})\text{max}} \approx \frac{U_{CC}}{R_3} \quad (3.35)$$



## 4. PCB Design

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### 4.1. General Assumptions

#### 4.1.a. Electrical schematic of the board

Not all the elements shown in Fig. 14 (p. 33) will be found on the PCB, which results, among others, from the design goals (see Chapter 2). Circuit schematic limited to the elements found on the board is presented in Fig. 18 (p. 44) for the full option and in Fig. 19 for the basic option.

The following changes have been introduced with respect to the full schematic of Fig. 14:

- in the full option, the transformer has been removed as it is found outside the board; instead, the connector (a terminal block)  $J_1$  has been provided to bring the voltage  $u_{\text{sec}}$  from the secondary winding;
- in the basic option, the transformer and the supply block (the rectifier and the control block supply) as they will be found outside the board; instead, the connector (a terminal block)  $J_2$  has been provided to bring the power supply ( $u_i$ ,  $u_{\text{CC}}$  and the common ground);
- the terminals of the potentiometer  $R_4$  have been highlighted to emphasize that this element can be located outside the board, connected using three separate wires;
- the halogen lamp  $L_h$  has been removed as it is found outside the board; the connector  $J_3$  has been provided instead to enable its connection;
- the measurement point  $P_0$  has been added to which oscilloscope probes' grounds are intended to be connected—in this place, a vertical stiff bare wire or a horizontal bare wire of an appropriate length should be soldered.

The final component list is presented in Table 3 (p. 46). The following data are provided:

- component symbol in accordance with Figs. 14, 18 and 19,
- the option in which the component is used,
- component kind,

- type, value, other parameters of the component,
- case type or its parameters,
- a sketch of case dimensions and basic lead arrangement on the universal PCB (white squares represent solder holes and pads),
- lead spacing (a minimum and a maximum one if there is a possibility to bend or cut off lead fragments).

Typical cases for components that will be used are presented in Fig. 17.

#### 4.1.b. Universal PCB used

In the present exercise, the UM-8 universal prototyping PCB may be used (see Section 1.1). Its image has already been shown in Fig. 1 (p. 8). The simplified trace and solder pads layout is shown in Fig. 16. The pitch of this board is 2.5 mm and its dimensions are 70 mm × 50 mm.

The UM-8 board is met in two sub-types. One of them has 10 full columns (i.e., where each vertical path has three holes) in either half; whereas the second one has 11 such columns. Fig. 16 corresponds to the sub-type with the lower column number. Both versions are implemented in the worksheet used in this exercise.

The information about the board sub-type used in a given year is published on the course web page together with worksheet description. In the case this information is not given when the design is begun, the design should be done for the board with 10 full columns. This will enable realising the design without any problem independent of which sub-type is received later. In the case of the 11-column sub-type one should only remember not to use the two opposite columns closest to the board centre.

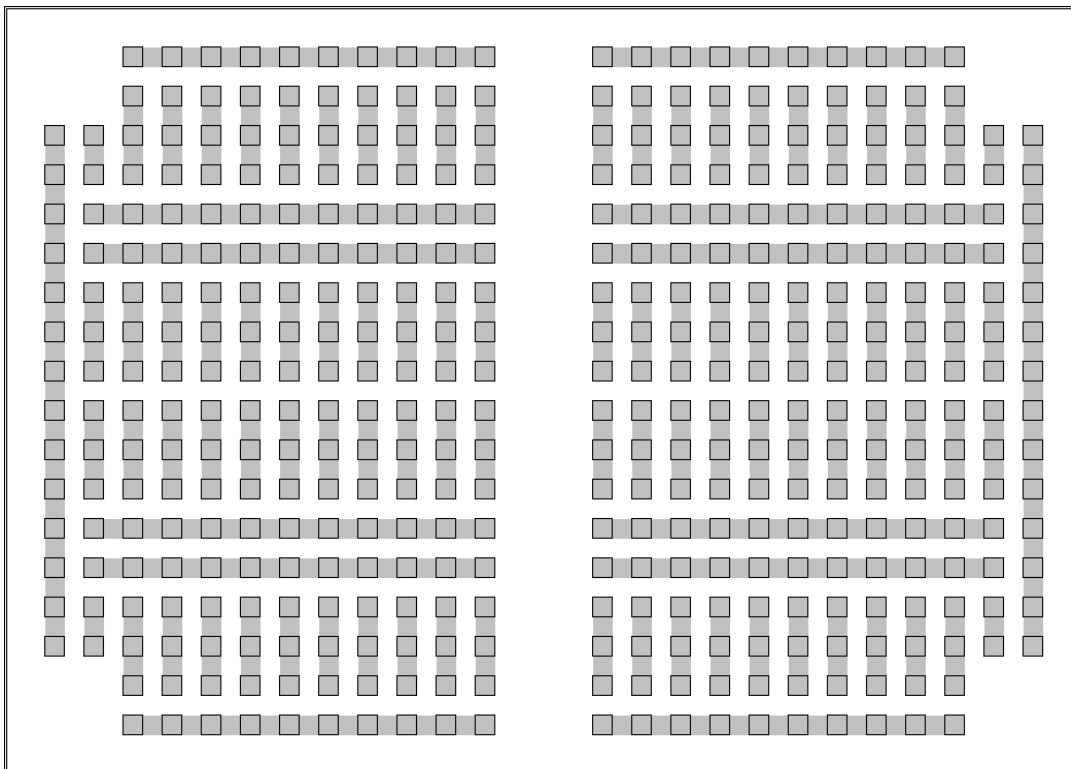


Fig. 16. A simplified image of conducting trace and solder pads layout for the UM-8 board with 10 full columns (squares with a black frame represent solder pads and grey areas represent conducting traces)



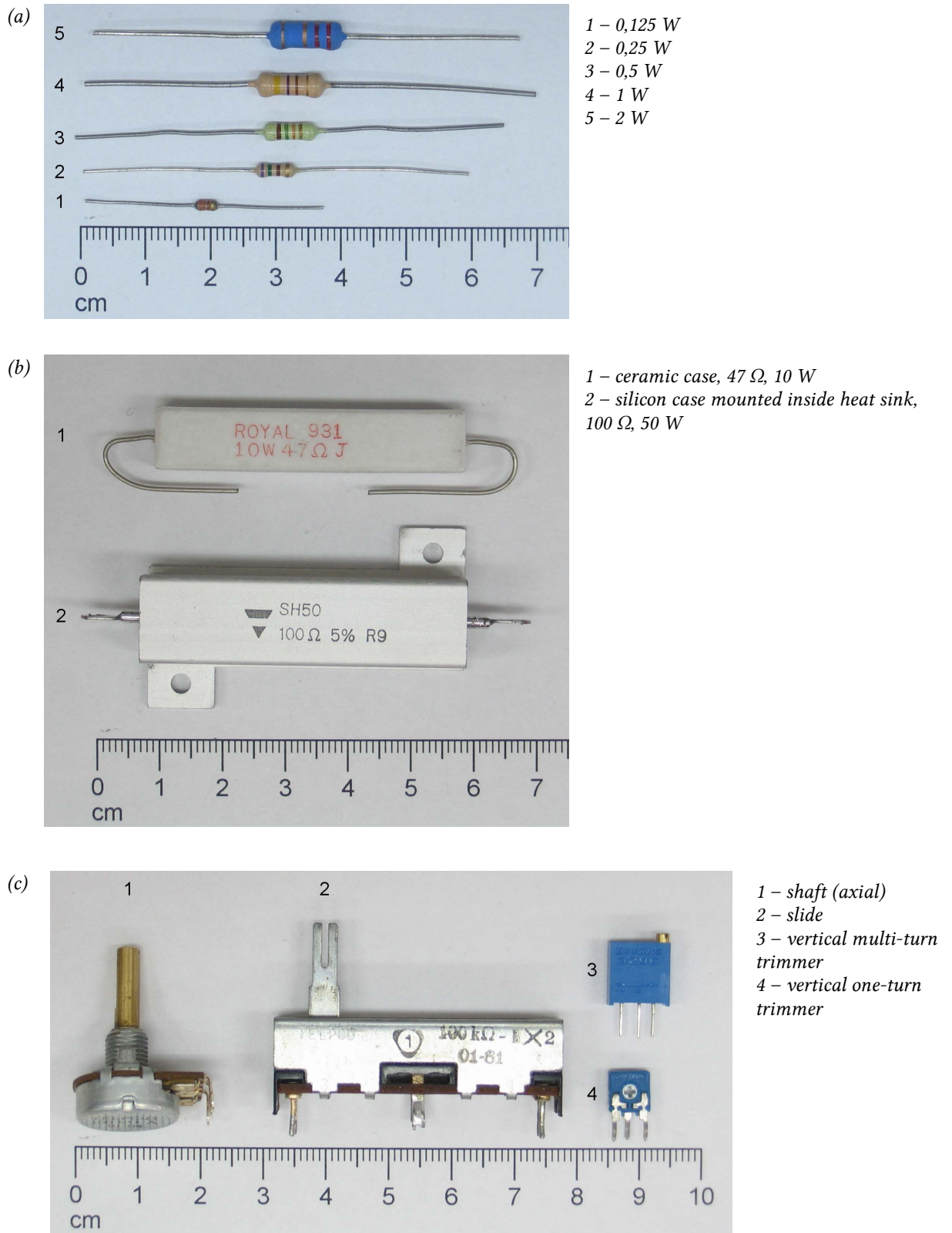


Fig. 17. Electronic components  
(a) low power resistors; (b) middle power resistors; (c) potentiometers

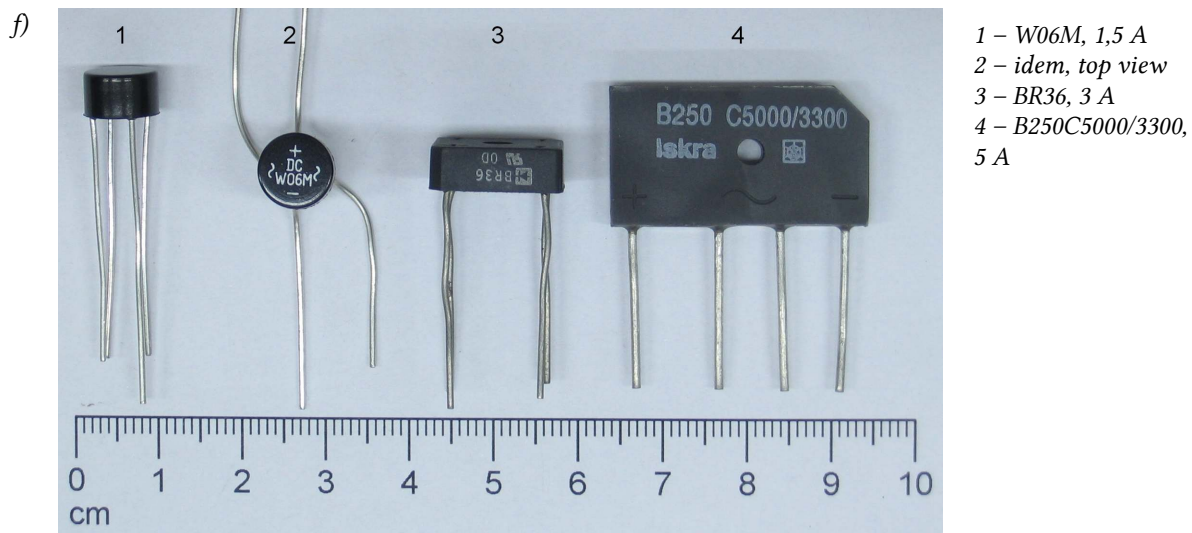
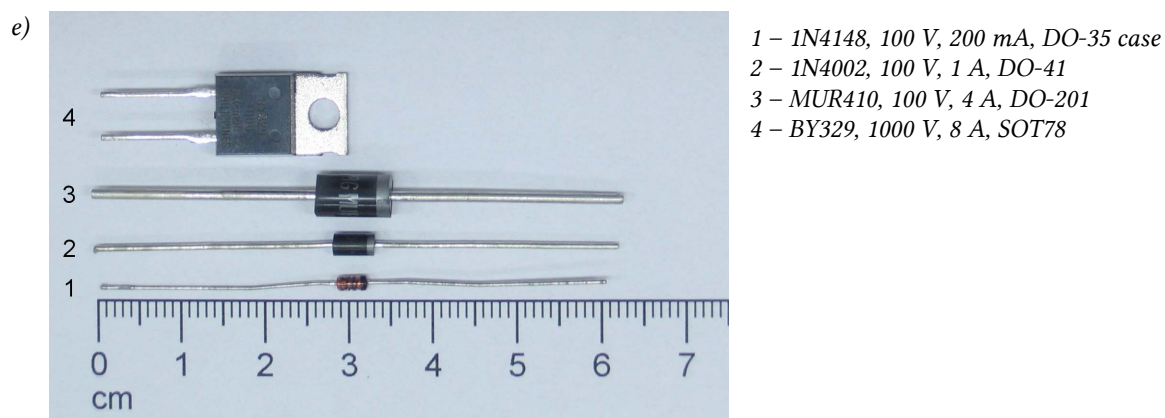
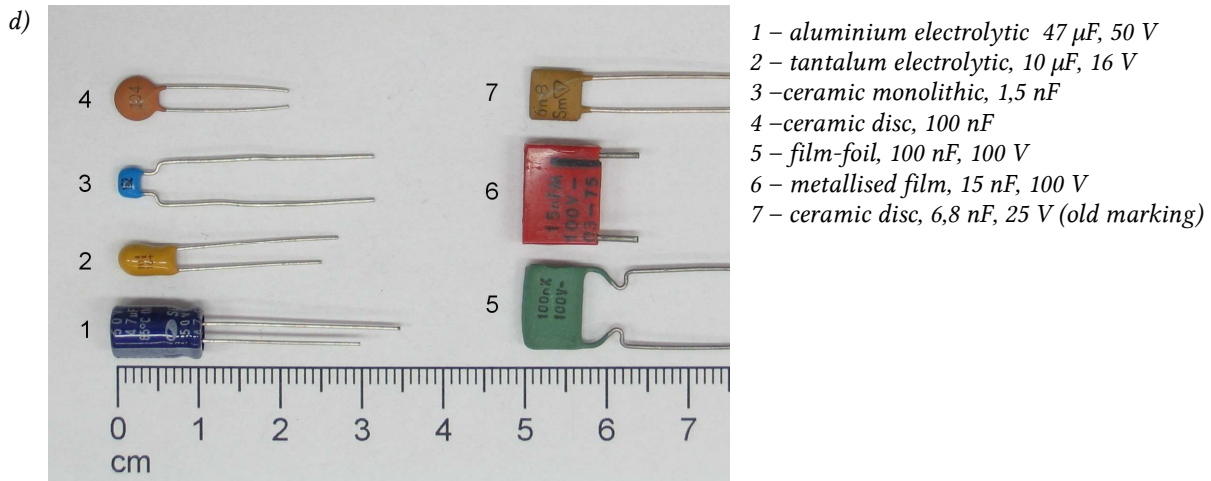


Fig. 17 (cont.) Electronic components  
 (d) capacitors; (e) diodes; (f) rectifier bridges

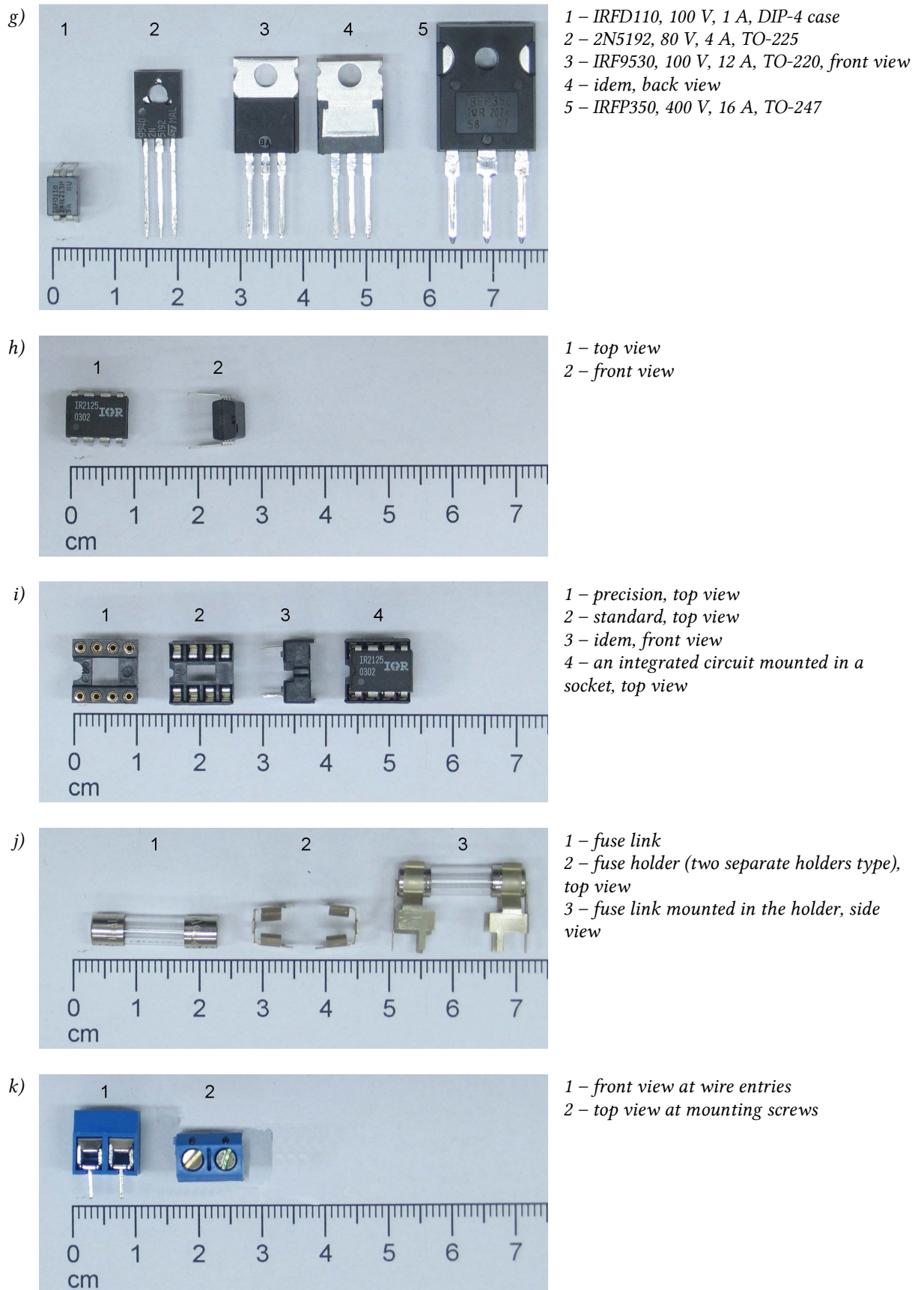


Fig. 17 (cont.) Electronic components

(g) power MOSFETs; (h) integrated circuit (IR2125, DIP-4 case); (i) integrated circuit socket; (j) IEC standard fuse (3,15 A, 250 V, 35 A breaking capacity); (k) terminal block, horizontal wire entry





Table 3. Component list

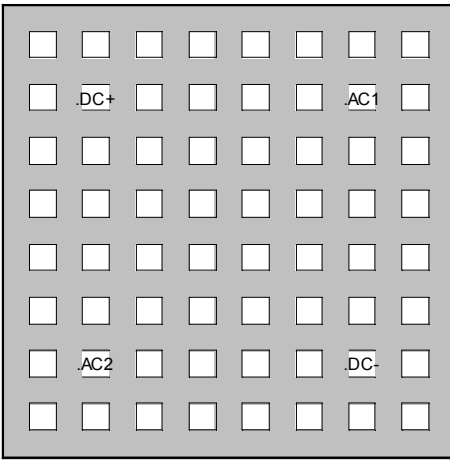
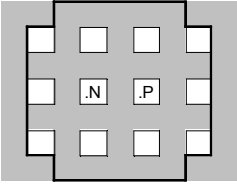
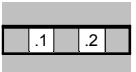
Symbol	Full Option	Basic Option	Component	Value Type Parameters	Case	Fig. 17 <sup>1</sup>	Sketch of Case Projection and Lead Arrangement on the Universal PCB	Lead Spacing
B <sub>1</sub>	●		Diode bridge, Graetz-type rectifying	KBPC10005 50 V, 10 A	Square <sup>2</sup>	f-3		5r <sup>3</sup>
C <sub>1</sub>	●		Capacitor, aluminium electrolytic	DZ, 105 °C	Vertical Dependent on value: min. ø 5, RM 2,5 max. (fig.) ø 8, RM 3,5	d-1		1r÷10r
C <sub>2</sub>	●		Capacitor, ceramic disc	100 nF, 50 V		d-4		1r÷8r

Table 3. Component list

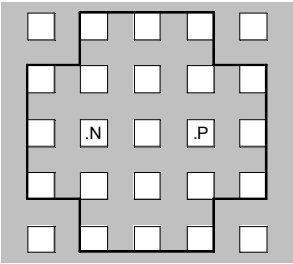
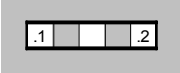


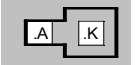
Symbol	Full Option	Basic Option	Component	Value Type Parameters	Case	Fig. 17 <sup>1</sup>	Sketch of Case Projection and Lead Arrangement on the Universal PCB	Lead Spacing
C <sub>3</sub>	●		Capacitor, aluminium electrolytic	DZ	Vertical Dependent on value: min. ø 6,3, RM 2,5 max. (fig.) ø 10, RM 5	d-1		1r÷10r
		●		10 µF, 25 V, 85 °C	Vertical ø 6,3, RM 2,5	d-1	Same as for C <sub>1</sub>	
C <sub>4</sub>	●	●	Capacitor, ceramic monolithic or film <sup>4</sup>	DZ	ceramic	d-3		(1r) 2r÷10r
					film	d-5		(2r) 3r÷20r
C <sub>5</sub>	●	●	Capacitor, ceramic disc	100 nF, 50 V		d-4	Same as for C <sub>2</sub>	
C <sub>6</sub>	●	●	Capacitor, ceramic disc	10 nF, 50 V		d-4	Same as for C <sub>2</sub>	
D <sub>1</sub>	●		Diode, power rectifying mains frequency	1N400x 1 A, 50 V (min)	DO-41 horizontal mount	e-2		4r÷18r
					vertical mount			1r÷4r

Table 3. Component list

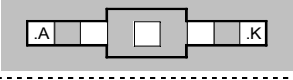
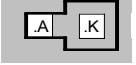
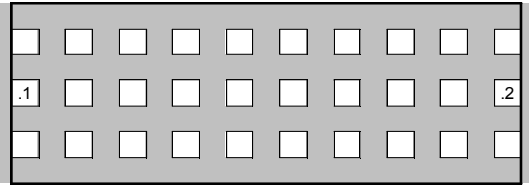
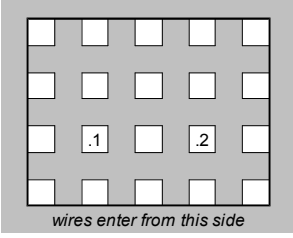
Symbol	Full Option	Basic Option	Component	Value Type Parameters	Case	Fig. 17 <sup>1</sup>	Sketch of Case Projection and Lead Arrangement on the Universal PCB	Lead Spacing
D <sub>2</sub>	●	●	Diode, small-signal fast switching	1N4148 200 mA, 100 V, 8 ns	DO-35 horizontal mount	e-1		4r ÷ 18r
					vertical mount			1r ÷ 4r
D <sub>3</sub>	●	●	Diode, power ultra-fast switching	UF400x 1 A, 50 V (min), 50 ns	DO-41	e-2	Same as for D <sub>1</sub>	
F <sub>1</sub>	●		Fuse link	DZ	5 mm × 20 mm	j-1	Mounted into the holder	
			Fuse holder			—		9r
J <sub>1</sub>	●		Terminal block, horizontal wire entry	2 poles	RM 5	k		2r



Table 3. Component list

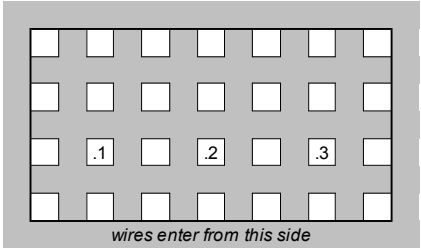

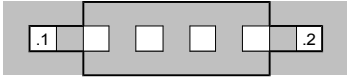
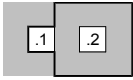
Symbol	Full Option	Basic Option	Component	Value Type Parameters	Case	Fig. 17 <sup>1</sup>	Sketch of Case Projection and Lead Arrangement on the Universal PCB	Lead Spacing
J <sub>2</sub>		●	Terminal block, horizontal wire entry	3 poles	RM 5	k <sup>5</sup>		$2 \times 2r$
J <sub>3</sub>	●	●	Terminal block, horizontal wire entry	2 poles	RM 5	k	Same as for J <sub>1</sub>	
P <sub>0</sub>	●	●	Measurement point			–		–
R <sub>3</sub>	●	●	Resistor, carbon	DZ, 0,125 W (min)	horizontal mount	a-2 a-3 a-4		$5r \div 20r$
					vertical mount			$1r \div 4r$

Table 3. Component list

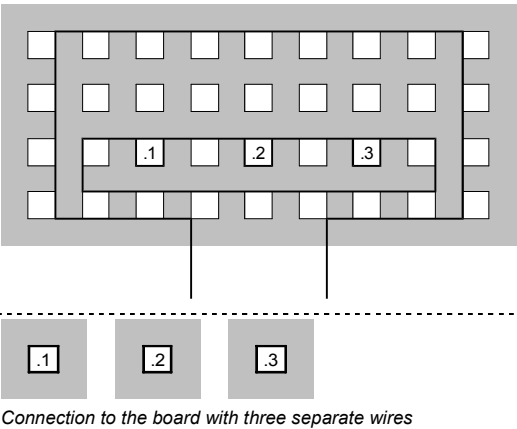
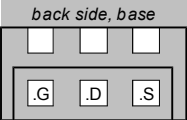
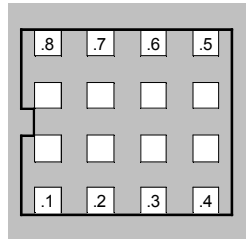
Symbol	Full Option	Basic Option	Component	Value Type Parameters	Case	Fig. 17 <sup>1</sup>	Sketch of Case Projection and Lead Arrangement on the Universal PCB	Lead Spacing
R <sub>4</sub>	●	●	Potentiometer, axial	DZ, linear	mounted at the board edge <sup>6</sup>	c-1		$2 \times 2r$  Any
R <sub>5</sub>	●	●	Resistor, carbon	DZ, 0,125 W (min)		a-3	Same as for R <sub>3</sub>	
R <sub>6</sub>	●	●	Resistor, carbon	DZ, 0,5 W (min)		a-3	Same as for R <sub>3</sub>	
R <sub>7</sub>	●	●	Resistor, carbon	10...100 kΩ, 0,125 W (min)		a-3	Same as for R <sub>3</sub>	
T <sub>1</sub>	●	●	MOSFET, power	According to design parameters	TO220AB (IR) <sup>6</sup>	g-3		$2 \times 1r^7$

Table 3. Component list

Symbol	Full Option	Basic Option	Component	Value Type Parameters	Case	Fig. 17 <sup>1</sup>	Sketch of Case Projection and Lead Arrangement on the Universal PCB	Lead Spacing
U <sub>1</sub>	●	●	Timer	NE555	DIP-8	h	Mounted in the socket	
			Integrated circuit socket	Standard	DIP-8	i-2		along X-axis $3 \times 1r$ along Y-axis $3r$

DZ – Selected by the team  
 $r$  – UM-8 universal PCB pitch = 2,5 mm  
 $\emptyset$  – Diameter in millimetres  
 RM – Lead pitch in millimetres

<sup>1</sup> The photograph depicts a case of identical shape, however dimensions can be different.

<sup>2</sup> The projection corresponds to the case body which is placed at ca. 10 mm above the board. On the board surface, only the mounting holes are occupied.

<sup>3</sup> Each lead can be bent in any direction by  $5r$  max.

<sup>4</sup> Distributed depending on stock; space should be provided for the bigger case.

<sup>5</sup> Same shape but different number of leads.

<sup>6</sup> The projection corresponds to the case body which is placed at least 4 mm above the board. The area corresponding to the inner contour may be assumed to be occupied on the board surface.

<sup>7</sup> Each lead can be bent forward or backward by  $2r$  max.; the G lead can be bent to the left by  $2r$  max.; the S lead can be bent to the right by  $2r$  max.



## 4.2. The real electrical character of connections

### 4.2.a. Effect of physical connections on circuit operation

Apart from the changes enumerated above, the new schematics are different from the one of Fig. 14 in one important aspect. They take into account (in the most important points) physical—not abstract—electrical connections.

In an abstract schematic we assume that each line symbolising an electrical connection is equipotential (a same electrical potential is present along its whole length) so it represents a short. In real circuits, especially when high and fast varying currents are flowing, it is not true. Each fragment  $\delta l$  of a conductor has some non-zero elementary resistance  $\delta R$  and some elementary inductance  $\delta L$ . The high current flowing through this conductor causes voltage drops to appear across these elementary resistances,

$$\delta u_R = \delta R \cdot i \quad (4.1)$$

and the fast variations of this current cause voltage drops to appear across the elementary inductances,

$$\delta u_L = \delta L \cdot \frac{di}{dt} \quad (4.2)$$

In power electronic circuits we deal with both, so important voltage drops may arise in the conductors.

Usually the drops across resistances are not high, so they do not have any negative effect on the operation of circuit components. On the contrary, voltage drops across inductances do, because they attain high values and short rise and fall times. Distortions of this kind have the potential of interfering with the operation of integrated circuits and discrete semiconductor devices.

For example, let's check the  $D_3$  diode. In Fig. 14 it has been connected in parallel with the  $L_h$  lamp. However, its purpose is to kill overvoltages occurring at the transistor's drain that result from voltage induced in the wires that are found between this drain and the positive end of the supply ( $u_i$  in the considered circuit). The very points of this diode's connection to the circuit are therefore a fundamental issue because if physical connections were made strictly according to Fig. 14, a substantial part of the wires would benefit from this diode action and would therefore still generate overvoltages observed at the drain  $\triangleright$  Exercise 6<sup>B</sup>. The schematic of Fig. 14 should obviously not be understood in such a literal manner as it is just an abstraction.

### 4.2.b. Schematic representation

The schematics of Figs. 18 and 19 are abstract, too. However, in the most crucial points they show what requirements should be met by physical connections on the board. This applies to the following issues.

1. Usually, diagonal ends of abstract wires indicate the necessity of connecting physical wires (leads, traces) directly to a given point. Staying with the example of the  $D_3$  diode, its ends should be soldered directly (the closest possible) to the drain of the transistor and to the positive end of the  $C_1$  capacitor, so that the drain potential cannot rise above the potential of the latter. The rest of the symbolic wires connecting the  $D_3$  diode are obviously still abstract. The schematic does not suggest then that the length of diode connections should be comparable to this of the whole power circuit. Quite the opposite, these should be the shortest possible.
2. Some wires, although equipotential as abstractions and apparently running in parallel (in the schematic), cannot be physically connected along their entire

length. An example may be the wire coming out from the GND pin of the  $U_1$  IC and heading downwards. It might appear that it can be directly connected to the wire running at the bottom which—as an abstraction—has the same potential (see Fig. 14). However, this bottom wire conducts the load current of high value and high rise and fall rates when the  $T_1$  transistor is switching. Thus, a fast varying voltage drop develops across this wire that would interfere with IC operation as potential of the GND pin is the reference potential for all its internal blocks. Any overvoltage or undervoltage at this pin can lead to e.g. erroneous comparator or latch operation.

For the above reasons, the load current should be conducted in a loop that is (along its longest possible fragment) disjoint from the IC supply loop. The GND pin should therefore not be inserted into the power circuit loop but directly connected to the  $C_3$  voltage stabilising capacitor.

#### 4.2.c. Specific requirements for connections

We will now point out the main requirements resulting from the abovementioned issues.

1. In order to reduce the level of disturbances generated in the high-current circuit loop, where steep current slopes occur, the associated stray inductance should be minimised. This loop (marked with circles in Figs. 18 i 19) should therefore be the shortest possible.
2. In order to effectively protect the drain from a potential rise above that of the positive end of the supply voltage ( $u_i$ ), the terminals of the clamping diode  $D_3$  should be mounted as close to the T1.D and C1.P (J2.1 in the basic option) pins as possible and any connections involved should be the shortest possible.
3. In order to effectively carry the disturbance-related charge appearing at the gate off to the supply ( $u_i$ ) ground, the  $R_7$  resistor should be mounted as close to the gate and source terminals of the  $T_1$  transistor as possible.
4. In order to reduce the level of disturbances that can be harmful for the transistor's gate circuit and for the IC, the gate circuit loop (marked with triangles), where also high and fast varying current flows, should have a minimum circumference and a minimum area enclosed, and should possibly not have any fragment common with the power circuit loop. The diagonal line indicates the necessity to directly connect U1.GND with T1.S, i.e. to realise a connection that does not have any fragments in common with the power circuit loop nor with other connections to U1.GND.
5. In order to efficiently carry off the disturbance-related charge and not allow it to pass to the IC, the  $C_5$  de-coupling capacitor should be mounted as close to the terminals U1.VCC and U1.GND as possible and any connections involved should be the shortest possible and realised without any additional wiring, using only the capacitor's leads.
6. Basically the same applies to the  $C_6$  capacitor, although it is not as critical as  $C_5$ . In order not to complicate the schematic, its connection has not been marked out graphically.
7. In order to ensure effective voltage stabilisation, the  $C_3$  and (in the full option)  $C_1$  capacitors should be mounted in such a way that the lines in and out are separated, i.e. that the diagonals drawn at different angles do not have any common fragments.
8. In order to ensure effective filtering of both low and high-frequency voltage variations, the  $C_1$  and  $C_2$  capacitors (in the full option) should be placed the closest possible one to another.
9. In order to prevent disturbances coming from the power circuit from affecting the supply of the logic part (the IC, especially), the connection of the negative end of the  $C_3$  capacitor with the negative end of the  $C_1$  capacitor (pin 3 of the  $J_2$

terminal block in the basic option) should not have any fragment in common with the power circuit loop.

10. In order to minimise the risk of disturbing the timer  $U_1$ , any path connected to the rapidly varying and relatively high drain voltage of the transistor (T1.D) should not be located in the immediate proximity of that integrated circuit.

The statement “should not have any fragment in common” should always be understood as aiming towards an ideal. In the reality, there will always be some common fragment, should it only be for the component’s own leads. We therefore tend to minimise the length of this fragment.

Design rules presented and discussed in Section 1.1.b still apply, too.

### 4.3. Realisation

Depending on the team's own skills, the design may be realised:

- (1) based on the universal prototyping PCB described in Section 4.1.b; you should then obey to the general rules presented in Section 1.1.b and to the remarks given below;
- (2) as a custom trace layout; in this case the PCB has not only to be designed but also etched (or realised using another technique) on your own *before* the first class on the present exercise.

During the realisation of the present exercise, the teacher is unable to organise stands and supervision necessary for PCB manufacturing. However, it is possible to use a drill and a laser printer in the laboratory.

**Custom designs should still keep component designations of Fig. 18 or 19, as applicable.**

In the case of circuits mounted on universal PCBs, it is not common to create a design on paper; the design is rather created on-the-fly, with the progress of soldering the consecutive elements. However, such an approach calls for some experience (otherwise, mistakes hard to localise are very likely to be made) and moreover, designs must be fast and credibly checked. For these reasons, the board should be designed and checked before circuit assembly begins. It is the purpose of the worksheet described in Sub-chapter 1.1 which includes a macro for automated design checking.

**Using the worksheet is not imperative. However, due to the lack of time, the teacher will not help finding errors in designs that have not been checked automatically.**

The worksheet version prepared for this laboratory contains:

- sheets named *UM\_8\_10* and *UM\_8\_11*, where the solder pads and conducting traces image of the UM-8 universal PCB in its 10 and 11-column sub-types, respectively, has already been entered (Fig. 16, see information in Section 4.1.b),
- sheets named *Pełny* and *Podstawowy*, where appropriate connection descriptions consistent with electrical schematics of the full (Fig. 18) and basic (Fig. 19) options, respectively, have been entered.

It is therefore not necessary to enter these data on one's own. Instead, right after opening the worksheet, you should:

- (1) make a copy of the *UM\_8\_10* or *UM\_8\_11* sheet—according to the board sub-type used (see Section 4.1.b)—and change its name to *Płytką* (exactly this one, with the Polish letter “ł”; you do not have to create the board image as told in the worksheet description);
- (2) change the name of the appropriate sheet—*Pełny* if you chose the full option or *Podstawowy* if you chose the basic option—to *Węzły schematu* (exactly, with Polish letters), after what the other sheet may be deleted (you do not have to create a node list as told in the worksheet description).



## Task 1. Component placement and connection planning on the PCB

Design a printed circuit board for the circuit to be prototyped. Irrespective of the chosen option (universal or custom PCB), the design should be accomplished according to the specific requirements given in Section 4.2.c.

In the case of universal PCB-based design, you should first of all get acquainted with information provided in Chapter 1. When using the worksheet, obey to the following detailed guidelines.

1. Distances between component leads must conform to the data shown in Table 3. Some elements (such as the fuse holder) have a fixed lead pitch; one value is then shown in the “Lead Spacing” column that corresponds to the sketch of the “Sketch of Case Projection and Lead Arrangement on the Universal PCB” column. In the case of others, some degree of arbitrariness exists; in the “Lead Spacing” column, minimum and maximum distances between leads are given then (see the footnotes, too). The sketch then corresponds to the initial (factory-made) or the least lead spacing.
2. It should be remembered that each component’s case has determinate geometrical dimensions and no other elements can be placed in the area occupied by it (see the “Sketch of Case Projection...” column) except when it is permitted in a footnote.
3. In the case of components whose case depends on design results (which is pointed out in the “Case” column), maximum possible case dimensions should be assumed. The sketch from the “Sketch of Case Projection...” column always corresponds to these maximum dimensions.
4. All the terminals in Figs. 18 i 19 have been labelled. Terminal labels entered into the sheet must follow the format: component\_name.terminal\_name, e.g. J1.2, B1.DC+, U1.7. Component and terminal names (labels) must be identical with those found in the schematic (Fig. 18 or 19).
5. Measurement points do not have terminals; only their names are to be entered into the sheet.
6. White colour (no cell fill) is reserved for pre-manufactured board traces. Additional connections that have to be realised using solder on the solder side, should be marked in a different colour (any except grey and red). Remember that erasing such connections is done by choosing “Light gray” (“Jasnoszary”) fill colour (not any other grey).
7. Supply and ground traces may be marked with any colour (except white, grey and red) if it helps you.
8. After design is completed, mark the power circuit loop (marked with circles in Figs. 18 and 19) with light red, and the gate circuit loop (marked with triangles in Figs. 18 and 19) with dark red.

Launch automated design check as described in the worksheet description attached. Modify the design if necessary.

After your design is accepted by the teacher, generate a horizontal flip of the board which will be useful during circuit assembly.



## 5. Electronic Design

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### 5.1. Introductory notes and calculations

#### Guidelines for task accomplishment

The aim of the tasks contained in this chapter is to select values or other parameters for some of the components of the circuit of Fig. 14 (p. 33): in the power supply block in the full option, and in the controller block in both options. It is good first to read each task in its entirety as useful explanations and hints may follow.

**The tasks applicable only for the full options have been marked with one asterisk while those applicable only to the basic option—with two asterisks.**

On some design stage it will be necessary to consider non-zero voltage drops in the real circuit, differently from the analysis that Fig. 13 (p. 30) has been based on. However, this figure will be helpful in understanding the general idea.

The necessary numerical data are found in:

- Table 2 on page 23,
- Table 3 on page 46,
- Table 4 below,
- and in the individual design parameters for a given team.

All calculations should be performed in the sequence presented in the report form where subsequent quantities are always arranged starting from the most original sources to the furthest results.

*Table 4. Additional circuit component data*

Transformer's secondary winding resistance	$R_{\text{sec}}$	0,55 $\Omega$
Voltage drop across the $F_1$ fuse at maximum load in the universal power supply for the basic option	$u_{F1(\text{max})}$	0,1 V
$C_3$ capacitor value in the universal power supply for the basic option	$C_3$	1 mF

## Task 2. Circuit characteristic values, upper estimate

Based on the circuit schematic (Fig. 14, p. 33) and circuit data given in Table 2 (p. 23), find upper estimates of the characteristic quantities describing the operation of the power circuit of the chopper: first, the amplitude of the input voltage  $U_{i(m)}$ , and next, the amplitude of the load current  $I_{o(m)}$  ➤ Exercises 2, 6<sup>A</sup>. „Amplitude” refers here to variations with the  $f_i$  frequency (see Fig. 13, p. 30).

Hints for voltage:

- Consider only the power circuit (disregard the control one) and disregard the presence of the  $C_1$ ,  $C_2$  filter.
- Assume that the mains voltage  $u_{sup}$ , and consequently, the secondary winding voltage  $u_{sec}$ , are ideal sinusoids. Using this assumption, calculate the amplitude  $U_{sec(m)}$  for the known rms value  $U_{sec(rms)}$ .
- There are no passive components between the  $u_{sec}$  and  $u_i$  voltages, so they attain their peak values both at the same moment (see Fig. 13).
- Assume that all the components are ideal, i.e. that conducting  $B_1$  bridge diodes and the  $F_1$  fuse have zero resistances. This is valid as under these assumptions there are no voltage drops along the path from the secondary winding ( $u_{sec}$ ) to the  $u_i$  voltage, so the  $u_i$  voltage will be the highest possible, so its maximum upper estimate will be obtained.

Hints for current:

- The amplitude of the load current  $i_o$  should be calculated based on the Ohm's law applied to the part of the circuit right of the  $u_i$  voltage.
- The  $i_o$  current flows when the  $T_1$  transistor is on.
- There are no passive components in the circuit right of  $u_i$ , so the  $u_i$  voltage and the  $i_o$  current attain their peak values both at the same moment (see Fig. 13).
- Assume that the  $T_1$  transistor is an ideal switch, i.e. it has a zero resistance in its on-state. This is valid, as under this assumption the current will be the highest, so its maximum upper estimate will be obtained.
- The halogen lamp resistance  $R_{Lh}$  should be calculated based on its nominal parameters ➤ Exercise 2.

### 5.3. Power supply operation

The tasks contained in this sub-chapter only apply to the basic option. The power supply design has been completed. It is however necessary to predict the effect of its operation so that transistor's gate circuit design, covered in sub-chapter 5.4, is possible.

Carrying out the following tasks is limited to using the formulae which have been given in their final form. It has also been made clear where to take parameter values from.

#### Task 7\*\*. Controller supply voltage: maximum estimation

Estimate the anticipated *maximum* value of the controller supply voltage  $U_{CC}$  and the *maximum* high level  $U_{GG(on)}$  of the generator's output voltage  $u_g$ . For this purpose, first estimate the *maximum* amplitude of the rectified voltage  $u_d$ .

Design formulae and usage sequence:

1. In order to obtain an *upper* estimate of the  $U_{CC}$  voltage, for the  $U_{d(m)}$  amplitude an *upper* estimate should also be found, so minimum voltage drops across components should be assumed. These will occur for minimum, i.e. zero, power circuit current ( $i_o = 0$ ). In such a case, it is only needed to overpass the threshold voltages  $U_{F(TO)}$  of the diodes found along the charging current path to charge the  $C_1$  capacitor. Thus

$$\begin{aligned} U_{d(m)\max} &= U_{\text{sec}(m)} - U_{F(TO),B1A} - U_{F(TO),B1D} = U_{\text{sec}(m)} - U_{F(TO),B1B} - U_{F(TO),B1C} = \\ &= U_{\text{sec}(m)} - 2U_{F(TO),B1} \end{aligned} \quad (5.2)$$

where  $U_{F(TO),B1}$  denotes the threshold voltage of a *single* diode in the  $B_1$  bridge.

2. The  $U_{CC}$  voltage will be the highest when the  $C_3$  capacitor is not discharged in any way (back through the  $D_1$  diode nor to the controller block meaning  $i_{\text{ctrl}} = 0$ ). Under this assumption, the  $U_{CC}$  voltage will keep the value it attains at the top of the  $u_d$  voltage. Thus it will be equal to the  $U_{d(m)}$  amplitude reduced by the voltage drop across the  $D_1$  diode:

$$U_{CC(\max)} = U_{d(m)\max} - U_{F(TO),D1} \quad (5.3)$$

Hints:

- The amplitude  $U_{\text{sec}(m)}$  of the secondary winding voltage  $u_{\text{sec}}$  has been calculated in Task 2.
- Threshold voltages are not given in data sheets for diodes used in this design. The typical value of 0,7 V will be a good estimate here.
- As follows from the NE555 timer description (Ref. [19]), the high level  $U_{GG(on)}$  of the generator's output voltage  $u_g$  is simply equal to the supply voltage  $U_{CC}$ . Although in the reality, a certain voltage drop will appear at the output of this integrated circuit, it is not possible to estimate it reliably at this point, so it should be neglected.

**Task 8\*\* . Rectified voltage: minimum amplitude estimation**

Estimate the *minimum* amplitude of the rectified voltage  $u_d$ . It is necessary to estimate the *minimum* value of the controller supply voltage  $U_{CC}$  in Task 9.

In order to obtain a lower estimate of the  $U_{d(m)}$  amplitude, maximum voltage drops across circuit components must be considered. These will occur for maximum currents flowing both in the power circuit and in the control circuit. It is also necessary to take the transistor's secondary winding stray (series) resistance  $R_{sec}$ . It can also be assumed that the current drawn by the control current is considerably lower than the principal current  $i_o$ , so only the principal current affects voltage drops across components of the power circuit. This leads to the following relationship.

Design formula:

$$U_{d(m)min} = U_{sec(m)} - I_{o(m)}R_{sec} - U_{F1}(I_{o(m)}) - 2U_{F,B1}(I_{o(m)}) \quad (5.4)$$

Hints:

- The upper estimate of the amplitude  $I_{o(m)}$  of the  $i_o$  current has been obtained in Task 2.
- The secondary winding series resistance  $R_{sec}$  is given in Table 4.
- The voltage drop  $U_{F,B1}$  across a *single* bridge diode for the appropriate current value should be read out of the static forward characteristic  $U_F = f(I_F)$  given in the bridge's data sheet.
- The voltage across a PIN diode, which is a bipolar device, is lowered when temperature rises. As justified above, maximum voltage drops should be estimated in this task. Therefore, the  $U_{F,B1}$  voltage should be read out of the characteristic for the lowest anticipated junction temperature  $T_j$ . As the circuit is intended for indoor use, this the typical value of 25 °C can be used.
- As can be stated based on Table 4, the maximum voltage drop  $u_{F1}$  across the  $F_1$  fuse is low as compared to other components, so it can be neglected.

**Task 9\*\*.** Controller supply voltage: minimum estimation

Estimate the *minimum* anticipated controller supply voltage  $U_{CC}$  and the *minimum* high level  $U_{GG(\text{on})}$  of the generator's output voltage  $u_g$ .

This task is limited to just subtracting the voltage drop across the  $D_1$  diode from the minimum value of  $U_{d(\text{m})}$  obtained in Task 8. In order to obtain a lower estimate for the  $U_{CC}$  voltage, maximum voltage drop must be considered which will occur for a maximum current drawn by the controller block and flowing through this diode.

Design formulae and usage sequence:

1. The charge drawn from the  $C_3$  capacitor during each period  $T_d$  of the rectified voltage  $u_d$ :

$$\Delta Q_{C3} = \Delta Q_{R3} + \Delta Q_{CC,U1} + \Delta Q_G = \frac{I_{R3(\text{av})\text{max}} + I_{CC(\text{max}),U1} + f_s Q_{G(\text{tot})}}{f_d} \quad (5.5)$$

Hints:

- For the auxiliary (external) circuitry for the  $U_1$  timer, a maximum average current  $I_{R3(\text{av})\text{max}}$  is included in the individual design parameters.
  - The supply current  $I_{CC}$  of the  $U_1$  integrated circuit is given in its data sheet. The maximum value should be chosen for a supply voltage  $U_{CC}$  closest to the maximum estimated in Task 7.
  - The total gate charge  $Q_{G(\text{tot})}$  should be read out of the gate charge characteristic  $U_{GS} = f(Q_G)$  given in the  $T_1$  transistor's data sheet ➤ Exercise 5<sup>A</sup>. The read-out should be done for a  $U_{GS}$  voltage equal to the maximum supply voltage  $U_{CC}$  estimated in Task 7 and for a  $U_{DS}$  voltage closest to the  $U_{i(\text{m})}$  amplitude according to the upper estimate from Task 2.
  - The frequency  $f_d$  of the rectified voltage  $u_d$  results from the circuit operating principle (see Section 3.2.b and Fig. 13), thus from the secondary winding (dimmer input) voltage frequency given in design parameters (Table 2, p. 23).
2. The change of the voltage across the  $C_3$  capacitor during one  $T_d$  period:

$$\Delta u_{C3} = \Delta u_{CC} = \frac{\Delta Q_{C3}}{C_3} \quad (5.6)$$

Hint:

- The value of  $C_3$  in the universal power supply that will be used for the basic option is given in Table 4 (p. 59).
3. The flow duration of the  $C_3$  capacitor charging current (so the  $D_1$  diode current) during each  $T_d$  period:

$$\Delta t_{\text{cond},D1} = \frac{1}{f_d} \left[ 1 - \frac{2}{\pi} \arcsin \left( 1 - \frac{\Delta u_{CC}}{u_{CC(\text{pk})}} \right) \right] \quad (5.7)$$

Hint:

- Instead of the unknown peak value  $u_{CC(\text{pk})}$  of the  $u_{CC}$  voltage, use the upper estimate of  $U_{CC}$  obtained in Task 7.
4. Maximum value of the  $D_1$  diode current

$$I_{D1(m)} = \frac{\pi}{2} \frac{\Delta Q_{C3}}{\Delta t_{\text{cond},D1}} \quad (5.8)$$

5. Minimum value of the controller supply voltage

$$U_{CC(\text{min})} = U_{d(m)\text{min}} - U_{F,D1}(I_{D1(m)}) - \Delta u_{CC} \quad (5.9)$$

Hints:

- For the minimum amplitude  $U_{d(m)\text{min}}$  of the  $u_d$  voltage, the estimate obtained in Task 8 should be used.
  - The voltage drop  $U_{F,D1}$  across the  $D_1$  diode for the appropriate, i.e. maximum  $I_{D1(m)}$ , current value should be read out from the static forward characteristic  $I_F = f(U_F)$  given in this diode's data sheet.
6. The minimum value of the high level of the gate driving voltage  $u_g$ :

Hint:

- Just as in Task 7, assume that the  $U_{GG(\text{on})}$  level is equal to the supply voltage  $U_{CC}$ .



## 5.4. Controller

Controller design is composed of two parts: pulse wave generator design (Tasks 10 to 11) and gate circuit design which reduces to calculation of the gate resistor  $R_6$  value appropriate for obtaining the required transistor turn-on time  $t_r$  (Task 12).

### Task 10. Pulse wave generator: calculations

Using the formulae derived for the modified astable circuit (sub-chapter 1.1), select values for the  $R_3$ ,  $R_4$ ,  $R_5$  and  $C_4$  components so that simultaneously:

- 1) the required frequency  $f_p$  of the  $u_g$  pulse waveform (at the OUT output of the  $U_1$  integrated circuit) is obtained,
- 2) the variation of the  $u_g$  waveform duty cycle is limited to the required range from  $D_{\min}$  to  $D_{\max}$ ,
- 3) the average (for the  $T_p$  period) current drawn by the auxiliary circuit ( $R_3$ ,  $R_4$ ,  $R_5$ ,  $C_4$ ) of the generator is limited to the required  $I_{R3(av)\max}$  value (the designation  $I_{R3}$  results from the fact that this current flows through the  $R_3$  resistor).

After a precise value is calculated, the results obtained should be aligned to the preferred number series (see Ref. [20]):

- $R_4$ : E3,
- $R_3$  and  $R_5$ : E12,
- $C_4$ : E6.

For design verification and further assembly, it is useful to get acquainted with the operating principle of the pulse wave generator described in Ref. [19] and Sub-chapter 1.1.

The sequence of operations should be as follows.

1. Calculate the minimum  $R_3$  value assuring that the required maximum average current  $I_{R3(av)\max}$  is not exceeded—formula (3.35).

Hints:

- Considering the requirement of not exceeding the given current value, the worst case will appear for a maximum supply voltage  $U_{CC}$  as the considered current will also be maximal.
- The maximum  $U_{CC}$  voltage has been determined in Task 6 (full option,  $D = 0$  case) or estimated in Task 7 (basic option,  $i_o = 0$  case).
- The  $R_3$  value should not be aligned to its preferred number series as it would introduce an inaccuracy that would propagate to further results.

2. From the formulae (3.29) and (3.30), based on the  $D_{\min}$  and  $D_{\max}$  values as required in the individual design parameters, as well as the minimum  $R_3$  value calculated in step 1, calculate the values of  $R_4$  and  $R_5$ .

Hints:

- Use any method to solve the above system of two linear equations.

3. Align the values of  $R_3$ ,  $R_4$  and  $R_5$  in a reasonable way to the preferred number series indicated in the beginning (considering the reasons given in hints below is understood under “reasonable”).

Hints:

- As the least accurate series is used for the  $R_4$  potentiometer, you should start with this component and only after adjust the values of  $R_3$  and  $R_5$  that can be set with more accuracy.

- As follows from the relationship for the duty cycle, the alignment should not result in a considerable change of the mutual ratios of all the 3 resistances. Otherwise, it will not be possible to obtain the required values of  $D_{\min}$  and  $D_{\max}$ . This means that the values of  $R_3$  and  $R_5$  should not necessarily be aligned to the *nearest* preferred number.
  - The value of  $R_3$  permits to keep the current consumption below the maximum level required. It cannot be therefore aligned downwards (unless slightly) as this would cause an increase in the current drawn and thus failure to comply with the individual design parameters.
4. From formula (3.27), calculate the value of  $C_4$  needed to obtain the required frequency of the  $u_g$  waveform. Align it to the preferred number series indicated above.

Hints:

- The requirement for the switching frequency is not a maximum nor a maximum limit. Instead, the frequency obtained should be the closest possible to the required one. The alignment should be made appropriately.

### Task 11. Pulse wave generator verification

By means of simulation using the MicroSim package, verify the correctness of component value selection carried out in Task 10. For this purpose, the ready-to-use simulation model of the generator should be used contained in the *zad\_10.sch* file.

In the Schematics application, complete the circuit schematic by entering the component values calculated or used in Task 10. Complete all the component designations by replacing question marks with your team number.

Hints:

- Models used in the *zad\_10.sch* file correspond to the simulator version available through the course web page.
- In case the NE555 model used is missing in the simulator version used, place the *ne555\_eval* library files (after unpacking it) in the design folder. If this does not help, install this library using the procedure described on the course web page. Do not use other models of 555 components available in the simulator version used as such symbols can have different pin layout and models can correspond to another 555 circuit versions (e.g., the unipolar one) which can lead to results not conforming to reality.
- In case the 1N4148 diode model is missing, replace its symbol with any available in the simulator version used. In order to look up all the models that possibly fit, enter \*4148\* in the *Part Name* field in the *Draw > Get New Part* dialog box.
- In the POT component model, the VALUE parameter corresponds to the total resistance, while SET represents the current division ratio  $k$  resulting from the wiper position (see Section 3.3.a). When this component is inserted as in the *zad\_10.sch* schematic, the value of SET = 0 corresponds to a zero resistance of the upper section of the potentiometer, thus to the extreme top wiper position.
- The supply voltage source should have the value of  $U_{CC}$  as used in Task 10.

**In this task, all component designations must conform to Fig. 14 and end in the team's number (e.g. R3.99 for team 99). Otherwise, your results will be treated as cheated.**

Carry out a time (transient) analysis of the circuit (► Exercise 6<sup>A</sup>) for three positions of the potentiometer's wiper:

- middle ( $k = 0,5$ ),
- extreme top ( $k = 0$ ),
- extreme bottom ( $k = 1$ ),

and determine:

- the waveform of the voltage at the CTL pin—in each case, within the same time interval as for items (2) and (5);
- the waveform of the  $u_g$  voltage (at the OUT pin)—in each case;
- the frequency  $f_p$  of the  $u_g$  waveform—for the middle wiper position;
- the minimum and the maximum duty cycles  $D$  of the  $u_g$  voltage—for the appropriate extreme wiper positions;
- the waveform of the current drawn from the supply by the generator's auxiliary circuit  $i_{R3}$ —for either extreme position;
- the average value (over the  $T_p$  period)  $I_{R3(av)}$  of the  $i_{R3}$  waveform— for either extreme position, while placing the moving average waveform in a single plot together with the corresponding  $i_{R3}$  waveform.

**Results should be documented with plots for cases listed in the report form.**

## Hints:

- f. About a dozen of first periods should be disregarded in analysis because—as can be seen—circuit operation stabilises only after some time. This time will vary with the potentiometer setting.
- g. According to the operating principle described in [19], frequency and duty cycle are influenced by the reference levels for the two comparators, the higher one being equal to the voltage at the CTL pin and the lower one, to half the higher one. The voltage at the CTL pin will initially vary due to the charging process of the  $C_6$  capacitor. This voltage is therefore a good indicator for the steady state of the circuit.
- h. The AVG (or AVGX) function than enables determining an average value in the Probe application was already used in ► Exercise 6<sup>A</sup>.

State whether the circuit operates properly and fits the requirements as defined in the individual design parameters:

- 1° the waveform and levels of the output voltage according to the circuit operating principle described in [19] (“Astable Operation” section and Figure 14);
- 2° the range of the duty cycle  $D$  of the  $u_g$  waveform is as required with an acceptable deviation  $\Delta D \leq \pm 0,05$  (for each of the values  $D_{\min}$  and  $D_{\max}$ ), where

$$\Delta D = D_{\text{obtained}} - D_{\text{required}} \quad (5.10)$$

- 3° the frequency  $f_p$  of the  $u_g$  waveform is as required with an acceptable relative deviation  $\Delta f_p / f_p \leq \pm 20\%$ , where

$$\frac{\Delta f_p}{f_p} = \frac{f_{p,\text{obtained}} - f_{p,\text{required}}}{f_{p,\text{required}}} \quad (5.11)$$

- 4° the average value of the current drawn by the generator’s auxiliary circuit  $I_{R3(\text{av})}$ , below the required maximum level of  $I_{R3(\text{av})\text{max}}$  in the worst case.

If discrepancies are detected, check the course of calculations done in Task 10 and verify alignment to the preferred numbers series. Introduce the necessary modifications and repeat the simulations.

## Task 12. Transistor's gate circuit

Calculate the *maximum* resistance of the gate resistor  $R_g$  ensuring that the *maximum* required rise time  $t_{r(\max)}$  is not exceeded. Use data included in the transistor's data sheet as well as on transistor's operating conditions estimations made in previous tasks. Align the calculated value to the E6 preferred number series.

All the design formulae needed have been given at the end of this task. They are approximate relationships, valid for a resistive load. In the circuit being designed, the load does not include any inductance (except for stray ones) and the current in the power circuit does not flow before the transistor is turned on and stops flowing after it is turned off. Therefore, the load is indeed resistive.

Hints:

- In the design formulae,  $R_G$  denotes the total resistance in the gate circuit. It is composed of the  $R_g$  resistor value, an internal gate resistance and an output resistance of the  $U_1$  integrated circuit. However, it is justified to assume that the latter two are much less than the first and thus

$$R_G \approx R_g \quad (5.12)$$

- The parameter that connects the control circuit (the gate resistance  $R_G$ ) and the principal circuit in respect of the switching times  $t_r$  and  $t_f$  is the charge delivered to a transistor's gate during the plateau (flat) section of the gate charge characteristic  $Q_G = f(U_{GS})$ , which follows from the measurement principle of this characteristic. The abovementioned charge is called the gate-drain charge  $Q_{GD}$  and it is the difference in the  $x(Q_G)$  coordinate between the beginning and the end of the said characteristic section ➤ Exercise 5<sup>A</sup>.
- For gate charge read-out, the guideline concerning the off-state  $U_{DS}$  voltage given in Task 6 (full option) or in Task 9 (basic option) still applies.
- The  $U_{GS(pl)}$  voltage is the plateau voltage or the level (the  $y$ , or  $U_{GS}$ , coordinate) of the flat section of the gate charge characteristic.
- As follows from Eq. (5.13), the rise time  $t_r$  increases when the high level  $U_{GG(on)}$  of the  $u_g$  voltage decreases. Thus, in view of obtaining the required *maximum* rise time, the worst conditions will occur for the *lowest*  $U_{GG(on)}$  value because it will be the most difficult to fit below the given limit of  $t_{r(\max)}$ .
- The minimum high level  $U_{GG(on)}$  of the  $u_g$  voltage has been estimated in Task 6 (full option) or in Task 9 (basic level).
- When aligning the  $R_g$  resistance to a preferred number series, remember that  $t_r$  increases with gate resistance ➤ Exercise 3<sup>A</sup>. Therefore, in order not to exceed the required maximum value of  $t_r$ , the  $R_g$  resistance cannot be higher than calculated (unless slightly).

Using the data sheet state whether it is possible to obtain the required rise time  $t_r$  using the specific gate driver which is the output of the  $U_1$  integrated circuit. For this purpose, calculate the gate current during the rise time period  $I_G(t_r)$  and compare with the current source capability (i.e. the capability of delivering current to the gate)  $I_{OUT(source)\max}$  given in the data sheet of the  $U_1$  integrated circuit. Calculate the gate current during the fall time period  $I_G(t_f)$  and compare with the current sink capability (i.e. the capability of taking current back from the gate)  $I_{OUT(sink)\max}$ . If needed, modify your design at the expense of decreasing the switching speed (increasing the rise time  $t_r$ ).

Hints:

- Use the final, i.e. aligned to a preferred number, value of  $R_g$  for calculations.
- As in the case of the high level  $U_{GG(on)}$ , assume that there is no voltage drop at the output of the  $U_1$  integrated circuit while in the low state. Thus, the GND pin potential is present at this output so the output voltage  $U_{GG(off)} = 0$ .

- j. In the NE555 integrated circuit data sheet enclosed, the current capability  $I_{OUT,max}$  should exceptionally be looked for within the general circuit description, not in the tables.

For the  $R_G$  value eventually obtained, calculate again the rise time  $t_r$  as well as the fall time  $t_f$ .

Design formulae:

$$t_r = \frac{R_G Q_{GD}}{U_{GG(on)} - U_{GS(pl)}} \quad (5.13)$$

$$t_f = \frac{R_G Q_{GD}}{U_{GS(pl)} - U_{GG(off)}} \quad (5.14)$$

$$I_G(t_r) = \frac{U_{GG(on)} - U_{GS(pl)}}{R_G} \quad (5.15)$$

$$I_G(t_f) = -\frac{U_{GS(pl)} - U_{GG(off)}}{R_G} \quad (5.16)$$

## 5.5. Semiconductor switch selection verification

Within a real design process, component selection takes an important part. In order to shorten the present exercise, this stage has been skipped as far as semiconductor devices (including integrated circuits) are concerned. Nevertheless, component selection and electrical schematic development usually form a loop that is repeated iteratively. This is because circuit ideas can be forced by specific components but also the choice of particular components can be forced by circuit topology and operating principle.

During a first course of the design loop, the designer does not have all the needed data. Let us consider the design process of the present exercise:

- before the electrical schematic has been developed, parameters describing the transistor's control circuit, such as gate drive voltage high level, could not be calculated;
- for this reason, switching times could not be determined;
- consequently, dynamic power loss could not be determined;
- therefore, it was not possible to state whether power loss was not higher than the maximum admissible one;
- so it was not possible to fully assess whether the selected transistor was appropriate for the circuit in development.

As soon as the electrical schematic becomes more elaborate, it is therefore necessary to re-iterate the design: go back to component selection and check whether they still fit the circuit.

In the present exercise, the above design stage has been restricted to the most important components and aspects:

- 1° verification of  $U_1$  integrated circuit operating conditions in respect of:
  - power supply  $U_{CC}$ , which has been already analysed within Tasks 5 and 6 for the full option, and is to be analysed for the basic option (Task 16),
  - load  $I_{OUT}$ , which has been already analysed in Task 12;
- 2° verification of actuator semiconductor switch  $T_1$  selection in respect of:
  - voltage safety of its principal circuit—Task 13,
  - thermal safety of its principal circuit—Tasks 14 and 15,
  - optimum control circuit operating conditions, which have been already analysed in Tasks 5 and 6 for the full option, and is to be analysed for the basic option (Task 16).

### Task 13. Transistor voltage rating

State whether the rated voltage  $U_{DSS}$  of the  $T_1$  transistor fulfils the selection rule-of-thumb with respect to the working (i.e., occurring during normal circuit operation) blocking voltage across the transistor  $U_{DS(off)}$  ➤ Exercise 6<sup>A</sup>.

Hints:

- a. While determining the  $U_{DS(off)}$  value, one should take into account that this voltage ( $u_{DS}$ ) varies periodically with the frequency of  $f_s$  (see the switch voltage  $u_{sw}$  waveform in Fig. 10, p. 26).
- b. As already noted, the voltage across the transistor in its blocking (off) state  $U_{DS(off)}$  equals the input (rectified) voltage  $u_i$ , so it varies periodically with the frequency of  $f_i$ .
- c. To assess transistor safety, a maximum  $U_{DS(off)}$  value should be used, which is the  $U_{i(m)}$  amplitude upper estimate obtained in Task 2.



## Task 14. Transistor power loss

Estimate the maximum amplitude of transistor average power loss  $P_{D(m,max)}$ . ‘Amplitude’ means the maximum value in time. ‘Maximum’ means the maximum value of this amplitude that can be obtained by changing the controlling quantity, i.e., the duty cycle  $D$ . The result will be used to assess transistor thermal safety in Task 15.

General hints:

- Power loss  $p_D$  varies in time for two reasons:  $T_1$  transistor switching with the  $f_s$  frequency (see Section 3.1.a) and periodic variations of the supply voltage  $u_i = u_d$  with the  $f_i$  frequency (see Section 3.2.b).
- The switching period  $T_s$  is much shorter than thermal time constants of the transistor and its case. Therefore, average power  $P_D$  over switching period  $T_s$  can be considered instead of the instantaneous power ➤ Exercise 6<sup>A</sup>.
- However, the  $T_i$  period of the  $u_i$  waveform is longer than the thermal time constants. Consequently, thermal effects of power loss being varying with the  $f_i$  frequency cannot be averaged. One should take into account that the average power  $P_D$ , i.e., the one averaged over the  $T_s$  period, still varies periodically with the  $T_i$  period, in connection with the  $u_i$  voltage. Thus, ‘amplitude’ relates to these variations.
- Static (on-state) power loss  $P_{D(stat)}$  and dynamic (turn-on and turn-off) average power loss  $P_{D(dyn)}$  must be considered ➤ Exercise 3<sup>A</sup>. Both these components vary periodically with the  $T_i$  period.
- For necessary formulae, see references for ➤ Exercise 3<sup>A</sup>. Split the total average power formula into a static and a dynamic part; then modify the static component formula so that the on-state resistance appears in it.

Common hints:

- As follows from appropriate formulae, average power loss is a function of the off-state voltage  $U_{DS(off)}$  and of the on-state current  $I_{D(on)}$ . As follows from Fig. 10 (p. 26), the first equals the input voltage  $u_i$  while the latter, the load current  $i_o$ .
- As noted above, it is not possible to disregard waveform variations with the  $f_i$  frequency. As both  $u_i$  and  $i_o$  waveforms attain their amplitudes in the same moment (see Fig. 13, p. 30), the average power loss  $P_D$  amplitude will also occur in this moment. Therefore, in order to estimate the *amplitude*  $P_{D(m)}$  of the average power loss, *amplitudes* of  $u_i$  and  $i_o$  waveforms, i.e.,  $U_{i(m)}$  and  $I_{o(m)}$  values, should be used.
- The upper estimates values (or even over-estimates) of  $U_{i(m)}$  and  $I_{o(m)}$  from Task 2 should be used.

Hints, static power loss:

- The  $T_s$  period is much shorter than the  $T_i$  period. Therefore, within one  $T_s$  period the values of  $u_i$  and  $i_o$  do not change significantly (in contrast to Fig. 13, where  $f_s$  frequency is only slightly greater than  $f_i$  for visibility reasons). Consequently, it can be assumed that the  $i_o$  current has a constant value of  $I_{o(m)}$  during all the on-time.
- The average static power loss in a MOSFET increases with increasing temperature ➤ Exercises 3<sup>A</sup>, 6<sup>A</sup>, 6<sup>B</sup>. Therefore, the *absolute maximum* junction temperature  $T_j$  should be used in calculations. This will affect on-state resistance  $R_{DS(on)}$  read-out from the transistor’s data sheet ➤ Exercise 3<sup>A</sup>.
- As follows from formulae, average static power loss is *maximum* for a *maximum* duty cycle value. Therefore,  $D = D_{max}$  should be used in calculations according to simulation results obtained in Task 11.

Hints, dynamic power loss:

- l. In the case of dynamic power loss, the resistive load character should be taken into account, which has been justified in Task 12.
- m. As noted in Task 5 (full option) or 7 (basic option), a change in the controlling quantity (the duty cycle  $D$ ) causes a change in the controller supply voltage  $U_{CC}$ , as voltage drops along the power circuit loops change. As pointed out in Task 12, this in turn causes a change in the rise time  $t_r$  (the lower the voltage, the longer the time). This fact must be taken into account, as dynamic power loss increases with increasing switching times ➤ Exercise 3<sup>A</sup>.
- n. Rise and fall times  $t_r$  and  $t_f$  for the gate resistance  $R_6$  finally established have been calculated in Task 12. They have been upper estimates as a minimum high level  $U_{GG(\text{on})}$  has been assumed (equal to the minimum value of  $U_{CC}$ ). This estimate can therefore be used in the present task.

### Task 15. Transistor thermal safety

Calculate the maximum admissible power loss  $P_{D(\max)}$  in the  $T_1$  transistor without an external heat sink. By comparison of the admissible value (“adm” subscript) to the anticipated working value (“wrk” index) calculated in Task 14 state if the device operates safely if no external heat sink is used.

Hints:

- a. For the necessary formula, see ➤ Exercise 6 .
- b. The switching frequency  $f_s$  fulfils the condition (➤ Exercise 6<sup>A</sup>) that enables considering average power  $P_D$ , i.e., the average over the  $T_s$  period, even if instantaneous power is a pulse wave in reality.
- c. However, calculations made using average power give results for average temperatures, while it is the maximum one that is necessary for assessment of transistor safe operation. This should be taken into account appropriately ➤ Exercise 6<sup>A</sup>.
- d. A final circuit would be enclosed in the lamp base, which would hinder heat exchange with the ambient. It should be therefore assumed that in room conditions, the transistor ambient temperature  $T_a$  can reach 40 °C.
- e. Remaining thermal parameters should be read out of the transistor’s data sheet ➤ Exercise 6<sup>A</sup>.

### Task 16\*\* . Control circuit operating conditions

By comparison to the appropriate data sheet parameters of the  $U_1$  integrated circuit check whether the estimated controller supply voltage  $U_{CC}$  guarantees proper operation of this circuit.

Hints:

- a. Maximum and minimum values of the controller supply voltage  $U_{CC}$  have been estimated in Tasks 7 and 9.
- b. In the NE555 integrated circuit data sheet, both an absolute maximum rating, whose exceeding may damage the circuit, and recommended operating conditions, for which proper continuous operation is guaranteed, are given for the supply voltage  $U_{CC}$ . From the design point of view, it is obviously necessary to assert proper continuous operation of the generator.

By comparison to the appropriate data sheet parameters of the  $T_1$  transistor check whether the high level  $U_{GG(\text{on})}$  of the gate driving voltage  $u_g$  guarantees with respect to the  $T_1$  transistor:

- 1° proper switching,

Hints:

- For proper transistor turn-on it is necessary that the drive voltage  $u_g$  (high level  $U_{GG(\text{on})}$ , see Fig. 13, p. 30) becomes higher than the transistor's threshold voltage  $U_{GS(\text{th})}$ .
- The threshold voltage  $U_{GS(\text{th})}$  exhibits some spread. A minimum and a maximum value are given in the datasheet that can be expected for a particular transistor item.
- For comparison, a  $U_{GS(\text{th})}$  value should be chosen such that comparison result tells whether *any* item will turn on properly when a  $U_{GS}$  voltage of *any*  $U_{GG(\text{on})}$  value from the estimated range is applied.
- According to the assumption from Task 12, the low level  $U_{GG(\text{off})}$  used to turn the transistor off is zero, which is surely less than the threshold voltage. Transistor proper turn-off is therefore asserted and does not have to be verified.

- 2° conduction of a maximum load current with a low output voltage, operating in the linear mode,

Hints:

- In order to state whether at a given  $U_{GS} = U_{GG(\text{on})}$  voltage the transistor is capable of conducting a given current, the static output characteristics  $I_D = f(U_{DS})$  for several  $U_{GS}$  values, given in the data sheet, should be analysed. ➤ Exercise 5<sup>A</sup>
- The upper estimate for  $I_{o(\text{m})}$  should be used as obtained in Task 2.
- The assessment of the 'low'  $U_{DS(\text{on})}$  value should be done visually. ➤ Exercise 5<sup>A</sup>

- 3° gate safety.

Hint:

- The data sheet gives an absolute maximum safe value for the gate-source voltage  $U_{GS}$ .

Hints:

- c. In all comparisons, an appropriate, i.e., the least favourable, estimate of the  $U_{GG(\text{on})}$  value should be used. An upper estimate has been obtained in Task 7 whereas a lower one, in Task 9.
- d. Transistor parameters and characteristics vary with temperature. The  $T_1$  transistor should properly fulfil its role as a switch under any conditions—both

at circuit start (room temperature) and after it heats up (when the temperature can become close to the absolute maximum one).

## 6. Exercise Realisation Rules

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1. The exercise may be realised as a full option (complete but more labour-consuming) or as a basic option (limited but possible to complete in a shorter time). Choosing the basic option does not have negative effect on exercise assessment. The team's choice may be changed during exercise realisation.

As an additional choice, electronic design may be realised in the basic option while board design and assembly may be realised in the full option. Component availability for teams that choose this combined option is not guaranteed.

In the manual, the following symbols are used:

- one asterisk (\*) denotes tasks that only apply to the full option,
  - two asterisks (\*\*) denote tasks that only apply to the basic option,
  - tasks without any asterisk apply for both options.
2. Each team carries out the design procedure for its own parameter set that is handed over by the teacher.
  3. The design should be carried out by oneself, according to the general schedule shown on the cover page of this manual and a detailed one handed over by the teacher. The team should start the design according to the schedule, anticipating that problems may arise that will require asking for teacher's advice. Consulting your teacher is possible during his office hours and—if only possible—after each class and at any other time agreed upon.
  4. Completing subsequent tasks should be documented with a report, which is a standard form filled in together, with any attachments listed in this form. The report, in an appropriate state of completion and with appropriate attachments, should be presented:
    - (a) to have the board design accepted—see the schedule (cover page),
    - (b) to have the electronic design accepted—see the schedule,
    - (c) to pass the exercise—as soon as the exercise (measurements) is completed or at any time in the future.
  5. Rules concerning the form of the printed circuit board are given in Section 4.3.

6. Components necessary for circuit prototyping (including the universal PCB) can be lent by the teacher after a deposit is paid in the amount of an average component cost according to current prices. The deposit is paid back as soon as all the received components are returned, de-soldered, working and in a state enabling their reuse, i.e., with a minimum lead length of 10 mm (only applicable to components with leads that can be shortened; 5 mm can be admitted in specific cases). Not returning the components does not have any consequence apart from the deposit not being paid back.

Components are handed in based on a list created on a standard form. A team member first signs the form after a first portion of components which are common for all the teams. Next, the team fills in the grey fields based on the approved electronic design, receives the remaining components and a member signs the form for a second time in the appropriate space.

It is also possible to use components purchased on one's own.

7. The Department provides soldering and testing hardware and materials.

It is also possible to use own tools, hardware and materials after notifying the teacher at the beginning of each class.

8. Soldering must be performed in the laboratory room, during scheduled sessions or additional sessions organised by teachers. In special cases, the teacher can allow part of the work to be done at home.

## 7. Expected Report Contents

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The report should be handed in in the paper form, prepared on a standard form filled in by hand. The form is available on the course web site. The report should contain results obtained after completing the tasks described in Chapters 4 and 5, according to the consecutive fields of the form. Attachments pointed out in the form should be enclosed in the paper form.

## 8. Required Knowledge

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### 8.1. Prerequisites

One should get acquainted with information provided in this manual. This knowledge will not be checked. However, lack of orientation in actions being carried out may cause problems with completing the exercise as well as consequences provided for in the laboratory regulations.

### 8.2. Test scope

Not applicable.

## 9. References

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