Universal PCB Design Support Worksheet
User's Manual

elaborated by Łukasz Starzak

The worksheet *plytka_uniwersalna.ods* enables designing and automatically checking a circuit design based on a universal prototyping Printed Circuit Board (PCB).

Universal PCB Entry

Before starting the design, you must create your universal PCB image in the sheet *Płytka*. This includes marking the laminate area and place solder pads and pre-manufactured conducting traces within it.

The **laminate area** is defined by drawing a rectangle with the fill colour of *Light gray* (*Jasnoszary*; no other grey can be used for this purpose). Such a laminate must have a border area along its edges, at least 1 cell thick, where nothing can be placed.

Solder pads are represented by cells filled with any colour else than *Light gray* or without any fill. It is suggested that unfilled cells with a black frame are used. Two pads not connecting on a real board must be separated in the sheet by at least one cell filled with *Light gray*. Otherwise they will be considered as mutually shorted.

Pre-manufactured connections are formed by stripes of adjacent cells (cells that touch one another by entire sides, not by corners) filled with any colour else than *Light gray* or without any fill. It is suggested that unfilled cells without a frame are used.

It is assumed that board and connections image are entered as seen from the top (component side).

Data Entry

Data entry consists in filling two sheets: *Węzły schematu* and *Płytka*.

Węzły schematu sheet and nodes list entry

A list of circuit's nodes is entered to the *Węzły schematu* sheet according to the circuit's electrical schematic. Each node is described in a separate row. There can be no empty rows between filled ones (a first empty row encountered is interpreted as the end of circuit's description).

A node description consists in listing labels of component terminals that meet in it. Terminal labels are entered side by side, each in a separate column. There can be no empty cells between filled ones (a first empty cells encountered is interpreted as the end of a node's description).

Płytka sheet, component placement and additional connections marking

Component placement consists in putting labels of component terminals in the *Płytka* sheet in places on conducting traces chosen by the designer.

Each terminal label may be placed in any cell filled with a colour else than *Light gray* or without any fill. However, it only makes practical sense to place them in those cells that have been marked as solder pads. An exception are components that the designer wishes to solder on the solder side.

Terminal labels entered in the *Płytka* sheet must be strictly consistent with those entered in the *Węzły schematu* sheet, so that future automated design check can be performed. Labels are case sensitive.

In a case where two or more terminals of a given elements are mutually galvanically connected (shorted) inside the component, this should be marked with a hash sign (#) at the end of the label. Otherwise such a connection will be ignored during design check.

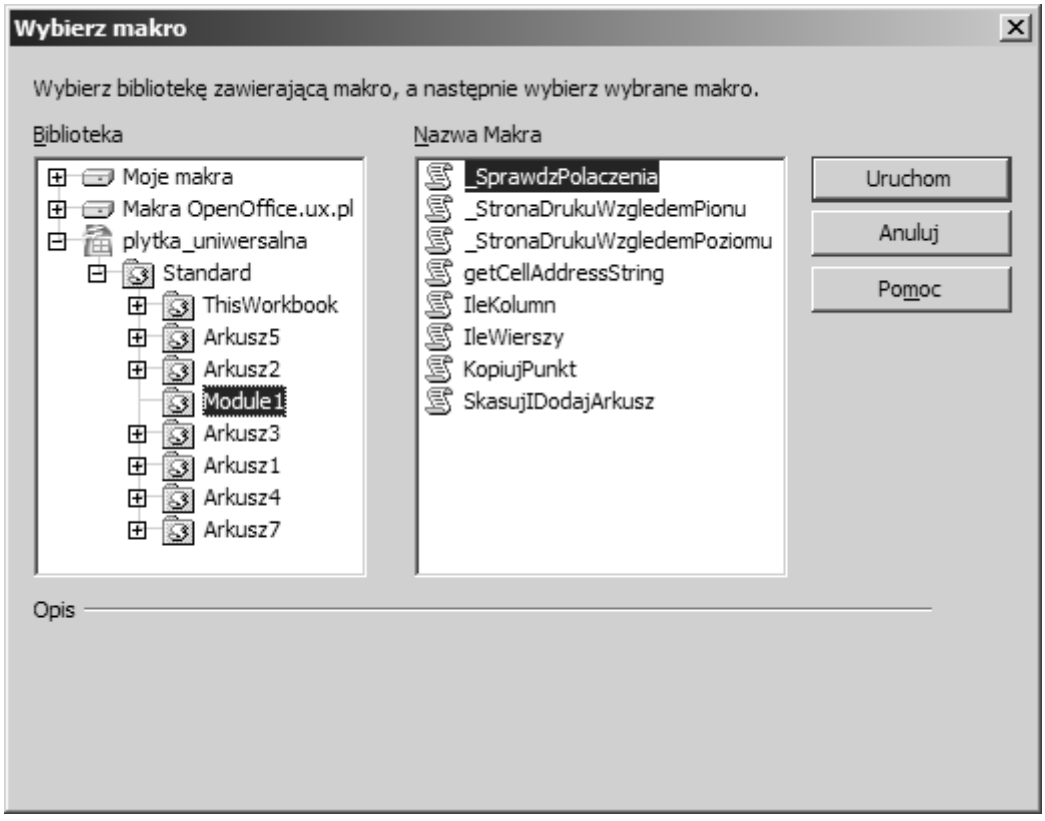
Unless they were listed in the *Węzły schematu* sheet, additional wire end labels should be preceded with a hash sign (#). Otherwise the board/schematic inconsistency error will be reported during design check.

If additional trace connections are to be realised using the solder on the solder side, they should be marked by changing the fill colour of the cell found between these traces, from *Light gray* to any other (using a colour different from the one used to mark pre-manufactured traces is suggested). Such a connection can be erased by reverting the colour to *Light gray*. The ends of such connections are not labelled.

Worksheet Functions

The worksheet provides the possibility to generate a mirrored PCB image as well as to verify the PCB design correctness using macros implemented therein. In order to run macros, it is necessary to first enable them from the menu *Tools*, *Options*, *LibreOffice*, *Security*, *Macro Security*, *Security Level* where at maximum *Medium* level should be selected.

Worksheet functions are launched from the dialog box that is open from the menu *Tools*, *Macros*, *Run Macro*. In the *Library* list (see picture below), unfold the *plytka_uniwersalna.ods* branch, then the *Standard* branch and click *Module1*. Next, in the *Macro Name* list select the appropriate macro name (see below) and confirm with *Run*. Macros that perform the worksheet functions have names that begin with and underscore (_). Other macros perform auxiliary tasks.



Mirrored board image

The worksheet offers the possibility to generate a mirrored PCB image. This function is useful for board assembly, enabling quick location of component terminals when the board is seen from the solder side.

In order to generate the image mirrored across the horizontal axis, the macro *_StronaDrukuWzgledemPoziomu* should be run.

In order to generate the image mirrored across the vertical axis, the macro *_StronaDrukuWzgledemPionu* should be run.

In both cases, the result will be put into a new sheet called *Strona druku*. (Warning: If there is an existing sheet with this name, it will be deleted and replaced with the new one.)

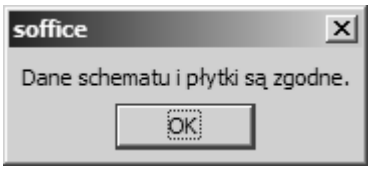
Design correctness check

Automated design check consists in comparing the connections resulting from the board image created in the *Płytka* sheet with those entered in the *Węzły schematu* sheet. It is started with the *_SprawdzPolaczenia* macro.

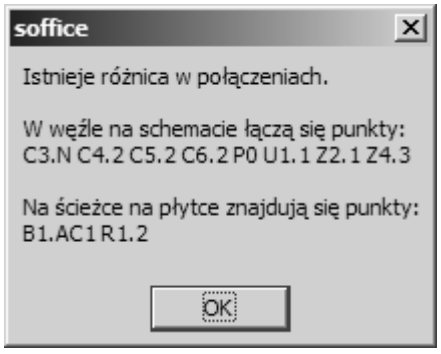
Design verification begins with sorting the list from the *Węzły schematu* sheet.

Next, an analogous list is generated and sorted based on the *Płytka* sheet. All component terminals placed on a same path (trace) will be handled as belonging to a same node. A path may be composed of several sub-paths connected by wires (terminals with names starting with a hash sign) or by internally shorted component terminals (terminals with names ending with a hash sign). A sub-path is formed by any group of adjacent cells (touching each other by sides) filled with a colour other than *Light gray* or without any fill.

In the end, both lists are compared. When they are fully consistent, the following message is displayed, meaning "Schematic and board data are consistent".



Otherwise, the first difference found between these lists is marked in red and the following error message is displayed, saying "A difference in connections exists". In its 3rd line, points (component terminals and wire ends) are listed that belong to a same node according to the schematic description entered in the *Węzły schematu* sheet. In its 5th line, points are listed that were found to be connected according to the board image created in the *Płytka* sheet.



In order to determine the reason for inconsistency of the two lists, it is best to start from finding in both lists marked in red these points that appear in only one of them. Next, check what other points they are connected to in the *Płytka* sheet.

If both lists are completely different, check which points listed in the *Weryfikacja płytki* sheet are shown as first (leftmost) in the board-based ("Płytka") rows and which—in the schematic-based ("Schemat") rows. If any of them appears on first position for the board only or for the schematic only, it means that this point has been mistakenly connected or has not been placed on the board at all, or has not been included in any node in the *Węzły schematu* sheet.