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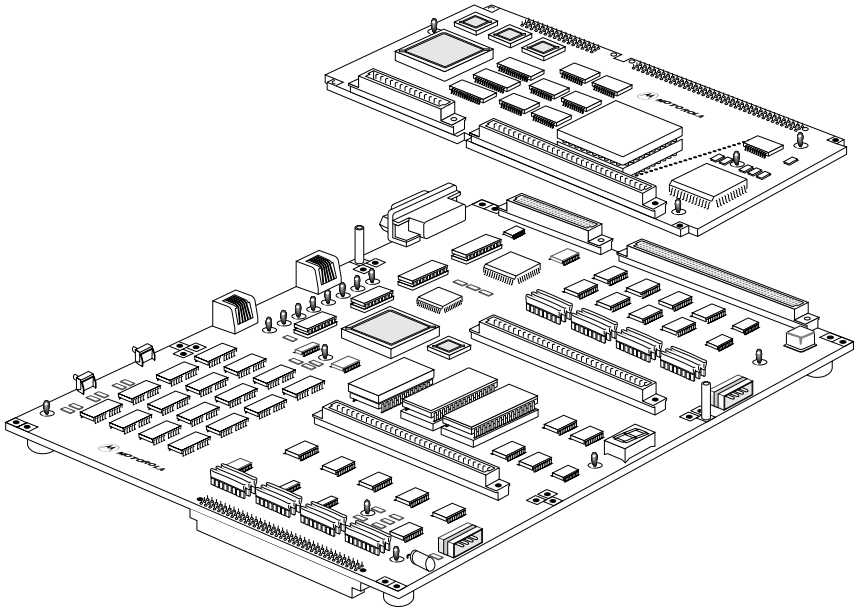
M68000IDP

Product Brief

M68000 Family Integrated Development Platform (IDP)

TheM68000 family IDP is a board set designed to provide a low-cost evaluation platform, yet flexible environment for developing both software and hardware for the family products. The platform provides the means for M68000 microprocessor and tool evaluation which enables users to properly select the microprocessor and associated tools for their next application. Because the turnkey development system requires the user to do very little to power up the system and begin development, significant time savings is realized by reducing the overall time that the product takes to get to market.

The IDP consists of an M68000 Family microprocessor-based CPU module as well as a generic IDP motherboard designed to support each CPU module. The IDP also includes two software debug monitor programs: Integrated Systems' ROM68K™ and Intermetrics' SmartROM™. This configuration allows the user to take advantage of an entire suite of features, including tracing, assembling, disassembling, and downloading, that are offered by the two monitors. Optional software is available to expand the development environment of the IDP by allowing the user to design, debug, and evaluate the M68000 microprocessor-based applications in real-time and non-real-time operating system environments. The IDP also functions as a tool for final test or fault analysis of user target systems.



M68000 Integrated Development Platform

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The IDP only requires a user-supplied power supply and an RS-232 ASCII terminal or host computer with an RS-232 serial port. Although the IDP will function using a terminal, the preferred communication device is a host computer. Operating the IDP with a host computer allows the user to develop, compile, and debug code using one of many optional software tools. Once code is developed, the program can be saved and downloaded to the IDP from the host computer.

IDP MOTHERBOARD

The IDP motherboard is a compact (10.7" x 7.5") printed circuit board. The motherboard is designed to accept any of the M68000 CPU modules and up to five input/output (I/O) modules. Functions provided by the IDP motherboard includes; bus routing and termination, power distribution, bus master and interrupt signal routing, serial and parallel I/O, clock calendar functions, and system memory. The IDP motherboard includes the following hardware features:

- One CPU Slot (M68000 Family CPU module)
- Five IDP Bus-Compatible I/O Slots
- Two RS-232 Serial I/O Channels
- IBM® PC/AT-Compatible Parallel Printer Port/24-Bit Timer
- Battery-Backed Clock/Calendar with 2040 Bytes SRAM
- Two 32-Pin EPROM Sockets, (Up to 512K x 16 EPROM)
- Two Mbytes of 5/2/2/2 Burst Mode DRAM

IDP BUS INTERFACE

The IDP provides a 32-bit data bus and a 28-bit address bus. Transfers take place synchronous to a 25-MHz clock, providing 36-Mbyte/sec sustained data rates.

The major features of the bus are as follows:

- 25-MHz Synchronous Operation
- 32-Bit Data Bus with Byte-Select Capability
- 28-Bit Address Bus for 16-Mbyte Direct Address Space to 16 Sections
- Individual Interrupt Request/Acknowledge Pair per I/O Slot
- Individual Bus Request/Acknowledge Pair per I/O Slot
- Maximum Data Rate of 36 Mbytes/Sec with 5/2/2/2 Burst Transfers

Five I/O expansion slots on the IDP motherboard enable the user to expand the I/O functionality of the IDP. In addition, I/O-related software can be used to take advantage of the added functionality. A variety of IDP bus-compatible I/O modules are available through third-party vendors. These modules include Ethernet, SCSI, IDE controller, and video controller cards. Additional information on the IDP bus interface can be obtained for users who want to design their own interface modules.

ROM MONITORS

Two monitor routines, ROM68K and MON68, reside in the ROM on the motherboard. The monitors provide the user with a generous set of commands for software development and debug. The IDP provides a convenient way to switch from one monitor to the other while maintaining a consistent development configuration.

The IDP boots with the ROM68K. The ROM68K features commands for reading and writing memory, viewing and/or changing CPU registers, assembling, disassembling, and downloading code via serial port or network connection. In addition, the monitor can be configured to automatically load a operating system from a host system and start it running when the target CPU is powered on or reset. Integrated Systems also offers pSOS+™, a real-time operating system, pROBE+™, a system-level debugger for pSOS+-based applications, and XRAY+™, a powerful source-evel debugger. XRAY+ and pROBE+ are highly integrated with the real-time operating system to allow the user to debug on an operating-system level as well as on a source level. Together, these development tools offer a complete real-time operating system solution for the user. XRAY+, pROBE+, and pSOS+ are offered as options with the IDP. The pSOS+ and pROBE+ are available through Motorola.

MON68 features commands to allow the user to set and display memory and registers. In addition, MON68 implements a trace function that allows the user to set breakpoints and examine traces of executed code. MON68 interfaces directly with Intermetrics' XDB™ source-level debugger. XDB's unique features include actual target-level access and direct control of program execution at the source statement or machine instruction level. The user can single step by source lines, machine instructions, and into and over procedure calls. XDB also has an assertion mechanism for testing a program under user-defined conditions. XDB is offered as an option with the IDP and can be obtained through Motorola.

Other compatible operating systems, compilers, and debuggers are offered by many third-party vendors, giving the user the option to tailor the development system specifically for his needs.

IDP MODES OF OPERATION

In addition to its use as a software development tool, the IDP can be used as a microprocessor evaluation tool as well as a hardware debugging tool depending on it's mode of operation. To accomplish this, the IDP contains a high-speed address translation table that gives the user the option to remap resources when using additional hardware that interfaces to the CPU local bus connector.

BYPASS MODE

Bypass mode is entered by default after a reset. In this mode, the address lines A12–A27 are routed directly through the output multiplexer and onto the IDP Bus. This is considered the normal mode of operation and is used when it is not necessary to remap IDP memory.

TRANSLATE MODE

In translate mode, CPU addresses A16–A27 form the input to the address translation map. The outputs of the translation table are routed via the output multiplexer onto IDP address lines A12–A27. In this mode, all addresses are translated. Using optional interface hardware attached to the IDP via the CPU local bus connectors, the user may plug into a target system CPU socket. This feature allows the user to debug the target system hardware while maintaining access to the IDP-based resources. The high-speed address translation map allows the user to map out portions of the IDP address space that conflict with the target. Bus arbitration and interrupt control may be software disabled, allowing those functions to be performed by target system circuitry.

EVALUATION

An optional high-speed memory board connected to the local bus connector provides a mechanism for measuring the performance of the microprocessor. The onboard memory can be configured so that the user

can emulate different types of memory (instruction or data areas) and different-sized devices (8-, 16-, or 32-bit widths). A software-selectable feature allows the user to designate areas of memory to have a specific number of wait states. In addition, dynamic bus sizing is supported by a feature that allows the user to specify different size configurations. A 32-bit onbaord timer provides profiling functionality. The user can monitor activities such as the total number of times certain areas of memory are accessed. Specifically the user can monitor the number of read accesses, the number of write accesses and the number of times the bus is utilized. These features provide a powerful tool to assist the user in selecting optimal processor/memory combinations prior to the actual design while considering important factors such as price/performance tradeoffs.

IDP CPU MODULE

The IDP CPU module is an IDP bus-compatible module based on an M68000 microprocessor. The CPU module is designed to be plugged into the IDP motherboard regardless of the microprocessor configuration. This design approach allows the user to target any of the 68K family by using the generic motherboard with any of the CPU modules. The CPU module provides the following features:

- M68000 Family MIcroprocessor
- Interrupt Control Circuitry
- IDP Bus Arbitration Circuitry
- Address Translation Map
- 16-Bit to 32-Bit Data Bus Translation (CPU000 only)
- Local Bus
- 25 MHz MC68882 Floating-Point Unit (CPU020, CPU030 only)

The CPU module has two DIN-style connectors. A 96-pin connector has signals that are the same or similar to the other CPU modules. The 48-pin connector has mostly the control and status signals that are unique to the specific CPU module. These signals are unbuffered and allow for the direct attachment of circuitry that cannot tolerate the delays imposed by the IDP bus.

Refer to M68000 CPU modules availability table on back page for CPU modules that are currently available.

M68000 CPU Module Availability

CPU	Available
MC68EC000*	—
MC68EC020*	—
MC68EC030	✔
MC68EC040*	—
MC68020*	—
MC68030*	—
MC68040*	—
MC68340*	—

*Contact your local Motorola sales office for future availability of these items.

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