eX Family FPGAs

Leading Edge Performance

- 240 MHz System Performance
- 4.2 ns Clock-to-Out (Pad-to-Pad)
- 330 MHz Internal Performance

Specifications

- 3,000 to 12,000 Available System Gates
- Up to 256 Dedicated Flip-Flops
- 0.22µ CMOS Process Technology
- Up to 132 User-Programmable I/O Pins

Features

- High-Performance, Low-Power Antifuse FPGA
- Very Low Power Consumption
- Very Low Standby Current (2mA)
- Low-Power Mode for Additional Power Savings (<250µA)
- Advanced Small-footprint Packages
- Hot-Swap Compliant I/Os
- Single-Chip Solution
- Nonvolatile
- Live on power up
- Power Up/Down Friendly (No Sequencing Required for Supply Voltages)
- Configurable Weak-Resistor Pull-up or Pull-down for Tristated Outputs at Power Up
- Individual Output Slew Rate Control
- 2.5V, 3.3V, and 5.0V Mixed Voltage Operation with 5.0V Input Tolerance and 5.0V Drive Strength
- Software Design Support with Actel Designer Series Tools
- Up to 100% Resource Utilization with 100% Pin Locking
- Deterministic Timing
- Unique In-System Diagnostic and Verification Capability with Silicon Explorer II
- Boundary Scan Testing in Compliance with IEEE Standard 1149.1 (JTAG)
- Secure Programming Technology Prevents Reverse Engineering and Design Theft

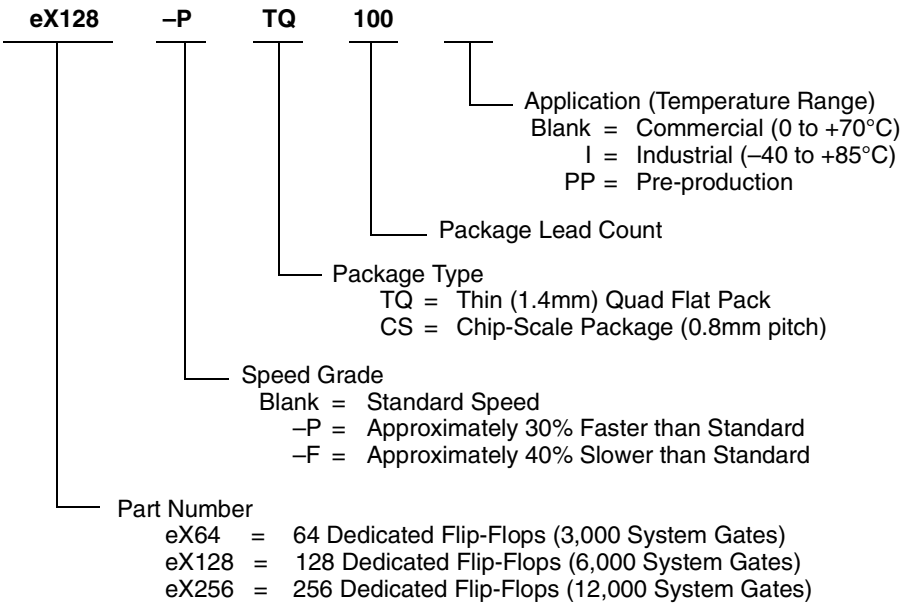
General Description

The eX family of FPGAs is a low-cost solution for low-power, high-performance designs. The inherent low power attributes of the antifuse technology, coupled with an additional low static power mode, make these devices ideal for power-sensitive applications. Fabricated with an advanced 0.22µ CMOS antifuse technology, these devices achieve high performance with no power penalty.

eX Product Profile

Device	eX64	eX128	eX256
Capacity			
System Gates	3,000	6,000	12,000
Typical Gates	2,000	4,000	8,000
Register Cells (Dedicated Flip-Flops)	64	128	256
Combinatorial Cells	128	256	512
Maximum User I/Os	84	100	132
Speed Grades	–F, Std, –P	–F, Std, –P	–F, Std, –P
Temperature Grades	C, I	C, I	C, I
Package (by pin count)			
TQFP	64, 100	64, 100	100
CSP	49, 128	49, 128	128, 180

Ordering Information



Product Plan

	Speed Grade*			Application	
	–F	Std	–P	C	I†
eX64 Device					
64-Pin Thin Quad Flat Pack (TQFP)	✔	✔	P	✔	P
100-Pin Thin Quad Flat Pack (TQFP)	✔	✔	P	✔	P
49-Pin Chip Scale Package (CSP)	P	P	P	P	P
128-Pin Chip Scale Package (CSP)	P	P	P	P	P
eX128 Device					
64-Pin Thin Quad Flat Pack (TQFP)	✔	✔	P	✔	P
100-Pin Thin Quad Flat Pack (TQFP)	✔	✔	P	✔	P
49-Pin Chip Scale Package (CSP)	P	P	P	P	P
128-Pin Chip Scale Package (CSP)	P	P	P	P	P
eX256 Device					
100-Pin Thin Quad Flat Pack (TQFP)	✔	✔	P	✔	P
128-Pin Chip Scale Package (CSP)	P	P	P	P	P
180-Pin Chip Scale Package (CSP)	P	P	P	P	P

Contact your Actel sales representative for product availability.

Applications: C = Commercial, I = Industrial

Availability: P = Planned, ✔ = Available

**Speed Grade: –P = Approx. 30% faster than Standard, –F = Approx. 40% slower than Standard*

† Only Std Speed Grade

Plastic Device Resources

Device	User I/Os (including clock buffers)				
	TQFP 64-Pin	TQFP 100-Pin	CSP 49-Pin	CSP 128-Pin	CSP 180-Pin
eX64	41	56	36	84	—
eX128	46	70	36	100	—
eX256	—	81	—	100	132

Contact your Actel sales representative for product availability.

Package Definitions: *TQFP = Thin Quad Flat Pack, CSP = Chip-Scale Package*

eX Family Architecture

The eX family architecture uses a "sea-of-modules" structure where the entire floor of the device is covered with a grid of logic modules with virtually no chip area lost to interconnect elements or routing. Interconnection among these logic modules is achieved using Actel's patented metal-to-metal programmable antifuse interconnect elements. Actel's eX family provides two types of logic modules, the register cell (R-cell) and the combinatorial cell (C-cell).

The R-cell contains a flip-flop featuring asynchronous clear, asynchronous preset, and clock enable (using the S0 and S1 lines) control signals (Figure 1). The R-cell registers feature programmable clock polarity selectable on a register-by-register basis. This provides additional flexibility while allowing mapping of synthesized functions into the eX FPGA. The clock source for the R-cell can be chosen from either the hard-wired clock or the routed clock.

The C-cell implements a range of combinatorial functions up to 5 inputs (Figure 2). Inclusion of the DB input and its associated inverter function dramatically increases the number of combinatorial functions that can be implemented in a single module from 800 options in previous architectures to more than 4,000 in the eX architecture.

Module Organization

Actel has arranged all C-cell and R-cell logic modules into horizontal banks called Clusters. The eX devices contain one type of Cluster, which contains two C-cells and one R-cell.

To increase design efficiency and device performance, Actel has further organized these modules into SuperClusters (Figure 3 on page 4). The eX devices contain type 1 SuperClusters, which are two-wide groupings of Type 1 clusters.

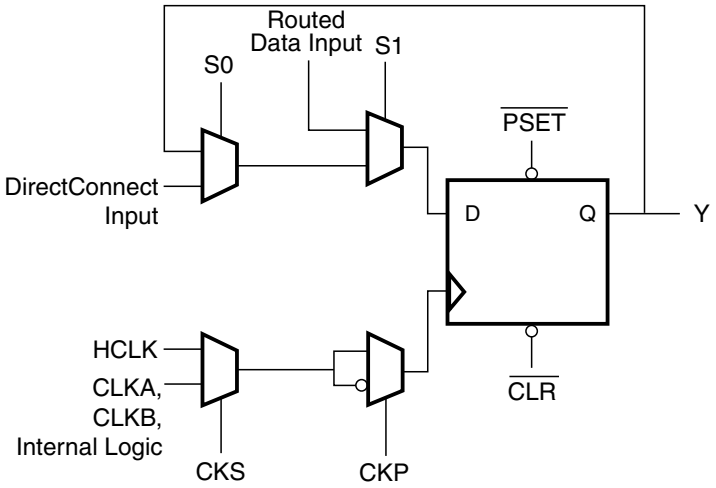


Figure 1 • R-Cell

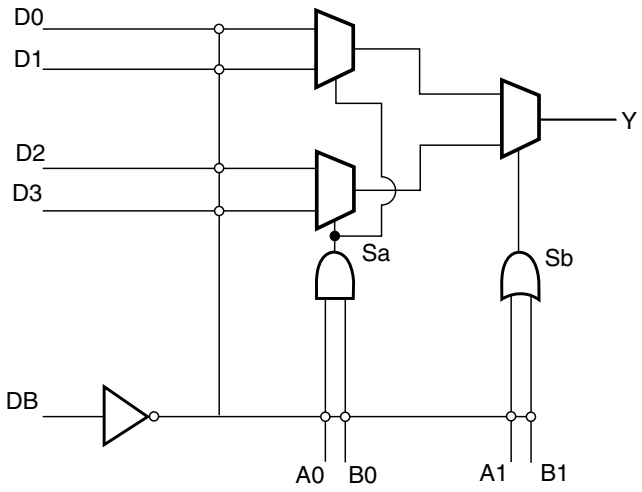


Figure 2 • C-Cell

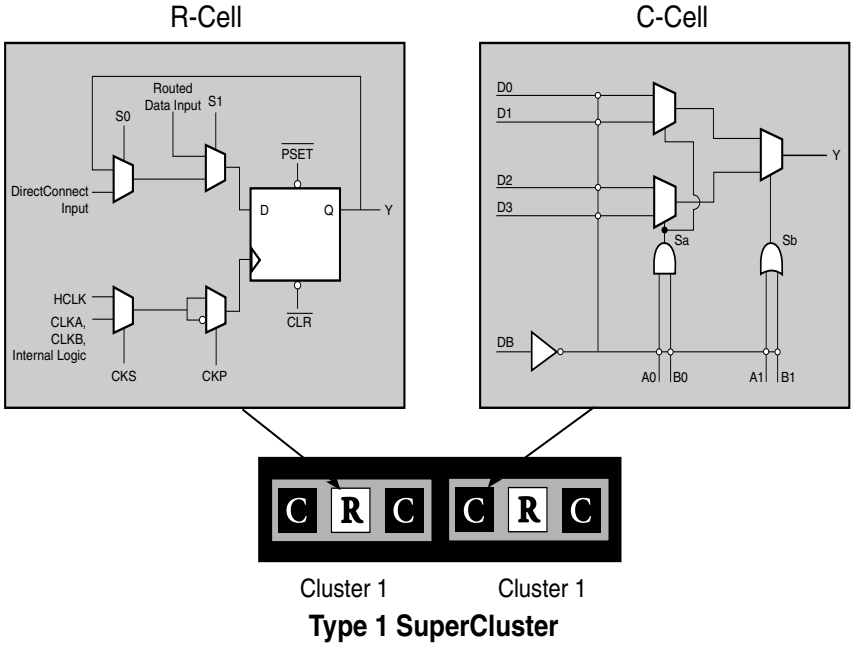


Figure 3 • *Cluster Organization*

Routing Resources

Clusters and SuperClusters can be connected through the use of two innovative local routing resources called FastConnect and DirectConnect, which enable extremely fast and predictable interconnection of modules within Clusters and SuperClusters (Figure 4). This routing architecture also dramatically reduces the number of antifuses required to complete a circuit, ensuring the highest possible performance.

DirectConnect is a horizontal routing resource that provides connections from a C-cell to its neighboring R-cell in a given SuperCluster. DirectConnect uses a hard-wired signal path requiring no programmable interconnection to achieve its fast signal propagation time of less than 0.1 ns.

FastConnect enables horizontal routing between any two logic modules within a given SuperCluster and vertical routing with the SuperCluster immediately below it. Only one programmable connection is used in a FastConnect path, delivering maximum pin-to-pin propagation of 0.3 ns.

In addition to DirectConnect and FastConnect, the architecture makes use of two globally oriented routing resources known as segmented routing and high-drive routing. Actel's segmented routing structure provides a variety of track lengths for extremely fast routing between SuperClusters. The exact combination of track lengths and antifuses within each path is chosen by the 100 percent automatic place-and-route software to minimize signal propagation delays.

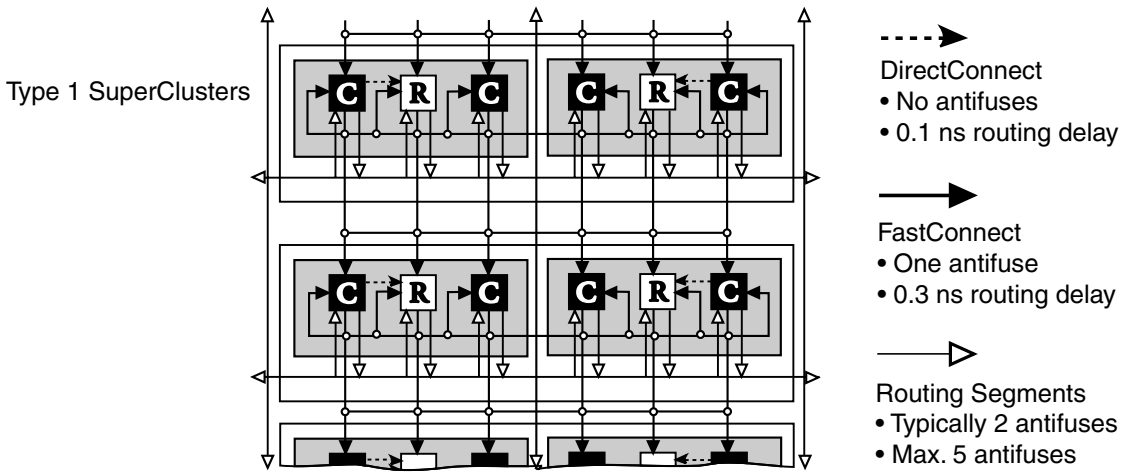


Figure 4 • *DirectConnect and FastConnect for Type 1 SuperClusters*

Clock Resources

Actel's high-drive routing structure provides three clock networks. The first clock, called HCLK, is hardwired from the HCLK buffer to the clock select MUX in each R-Cell. HCLK cannot be connected to combinational logic. This provides a fast propagation path for the clock signal, enabling the 4.2ns clock-to-out (pad-to-pad) performance of the eX devices. The hard-wired clock is tuned to provide clock skew is less than 0.1ns worst case.

The remaining two clocks (CLKA, CLKB) are global clocks that can be sourced from external pins or from internal logic signals within the eX device. CLKA and CLKB may be connected to sequential cells or to combinational logic. If CLKA or CLKB is sourced from internal logic signals then the external clock pin cannot be used for any other input and must be tied low or high. Figure 5 describes the clock circuit used for the constant load HCLK. Figure 6 describes the CLKA and CLKB circuit used in eX devices.

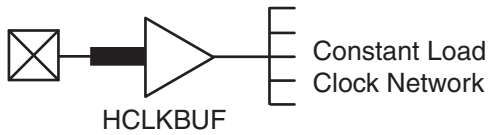


Figure 5 • eX HCLK Clock Pad

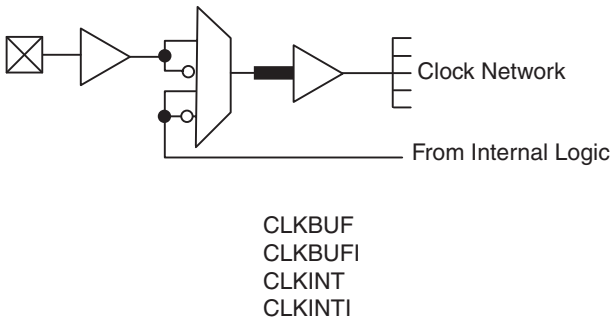


Figure 6 • eX Routed Clock Buffer

Other Architectural Features

Technology

Actel's eX family is implemented on a high-voltage twin-well CMOS process using 0.22µ design rules. The metal-to-metal antifuse is made up of a combination of amorphous silicon and dielectric material with barrier metals and has an "on" state resistance of 25Ω with a capacitance of 1.0 fF for low signal impedance.

Performance

The combination of architectural features described above enables eX devices to operate with internal clock frequencies exceeding 330 MHz for very fast execution of complex logic functions. Thus, the eX family is an optimal platform upon which to integrate the functionality previously contained in CPLDs. In addition, designs that previously would have required a gate array to meet performance goals can now be integrated into an eX device with dramatic improvements in cost and time to market. Using timing-driven place-and-route tools, designers can achieve highly deterministic device performance.

I/O Modules

Each I/O on an eX device can be configured as an input, an output, a tristate output, or a bidirectional pin. Even without the inclusion of dedicated I/O registers, these I/Os, in combination with array registers, can achieve clock-to-out (pad-to-pad) timing as fast as 4.2ns. I/O cells that have embedded latches and flip-flops require instantiation in HDL code; this is a design complication not encountered in eX FPGAs. Fast pin-to-pin timing ensures that the device will have little trouble interfacing with any other device in the system, which in turn enables parallel design of system components and reduces overall design time. See Table 1 for more information.

Table 1 • I/O Features

Function	Description
3 Level Selections	• 2.5V/3.3V LVTTL • 5.0V TTL • 5.0V TTL/CMOS*
Output Buffer	"Hot-Swap" Capability • I/O on an unpowered device does not sink current • Can be used for "cold-sparing" • Selectable on an individual I/O basis • Individually selectable low-slew option
Power Up	Individually selectable pull-ups and pull-downs during power up (default is to power up in tristate) Enables deterministic power up of device V_{CCA} and V_{CCI} can be powered in any order

Hot Swapping

eX I/Os are configured to be hot swappable. During power-up/down (or partial up/down), all I/Os are tristated. V_{CCA} and V_{CCI} do not have to be stable during power up/down, and they do not require a specific power-up or power-down sequence in order to avoid damage to the eX devices. After the eX device is plugged into an electrically active system, the device will not degrade the reliability of or cause damage to the host system. The device's output pins are driven to a high impedance state until normal chip operating conditions are reached. Please see Actel's web site for future Application Notes concerning Hot Swapping.

Power Requirements

The eX family supports mixed voltage operation and is designed to tolerate 5.0V inputs in each case (Table 2). Power consumption is extremely low due to the very short distances signals are required to travel to complete a circuit. Power requirements are further reduced because of the small number of low-resistance antifuses in the path. The antifuse architecture does not require active circuitry to hold a charge (as do SRAM or EPROM), making it the lowest-power architecture FPGA available today. Also, when the device is in low power mode, the clock pins must not float. They must be driven either HIGH or LOW. We recommend that signals driving the clock pins be fixed at HIGH or LOW rather than toggle to achieve maximum power efficiency.

Table 2 • Supply Voltages

	V_{CCA}	V_{CCI}	Maximum Input Tolerance	Maximum Output Drive
eX64 eX128 eX256	2.5V	2.5V	5.0V	2.5V
	2.5V	3.3V	5.0V	3.3V
	2.5V	5.0V	5.0V	5.0V

Low Power Mode

The new Actel eX family has been designed with a Low Power Mode. This feature, activated with a special LP pin, is particularly useful for battery-operated systems where battery life is a primary concern. In this mode, the core of the device is turned off and the device consumes minimal power with low standby current. In addition, all input buffers are turned off, and all outputs and bidirectional buffers are tristated when the device enters this mode. Since the core of the device is turned off, the states of the registers are lost. The device must be re-initialized when normal operating mode is achieved.

Boundary Scan Testing (BST)

All eX devices are IEEE 1149.1 compliant. eX devices offer superior diagnostic and testing capabilities by providing Boundary Scan Testing (BST) and probing capabilities. These functions are controlled through the special test pins in conjunction with the program fuse. The functionality of each pin is described in Table 3. In the dedicated test mode, TCK, TDI and TDO are dedicated pins and cannot be used as regular I/Os. In flexible mode, TMS should be set HIGH through a pull-up resistor of 10kΩ. TMS can be pulled LOW to initiate the test sequence.

Configuring Diagnostic Pins

The JTAG and Probe pins (TDI, TCK, TMS, TDO, PRA, and PRB) are placed in the desired mode by selecting the appropriate check boxes in the "Variation" dialog window. This dialog window is accessible through the Design Setup Wizard under the Tools menu in Actel's Designer software.

Table 3 • Boundary Scan Pin Functionality

Program Fuse Blown (Dedicated Test Mode)	Program Fuse Not Blown (Flexible Mode)
TCK, TDI, TDO are dedicated BST pins	TCK, TDI, TDO are flexible and may be used as I/Os
No need for pull-up resistor for TMS	Use a pull-up resistor of 10kΩ on TMS

TRST Pin

When the "Reserve JTAG Reset" box is checked (default setting in Designer software), the TRST pin will become a Boundary Scan Reset pin. In this mode, the TRST pin will function as an asynchronous, active-low input to initialize or reset the BST circuit. An internal pull-up resistor will be automatically enabled on the TRST pin.

The TRST pin will function as a user I/O when "Reserve JTAG Reset" box is not checked. The internal pull-up resistor will be disabled in this mode.

Dedicated Test Mode

When the "Reserve JTAG" box is checked, the eX is placed in Dedicated Test mode, which configures the TDI, TCK, and TDO pins for BST or in-circuit verification with Silicon Explorer II. An internal pull-up resistor is automatically enabled on both the TMS and TDI pins. In Dedicated test mode, TCK, TDI, and TDO are dedicated test pins and become unavailable for pin assignment in the Pin Editor. The TMS pin will function as specified in the IEEE 1149.1 (JTAG) Specification.

Flexible Mode

When the "Reserve JTAG" box is not selected (default setting in Designer software), the eX is placed in Flexible mode, which allows the TDI, TCK, and TDO pins to function as user I/Os or BST pins. In this mode the internal pull-up resistors on the TMS and TDI pins are disabled. An external 10K ohm pull-up resistor to VCCI is required on the TMS pin.

The TDI, TCK, and TDO pins are transformed from user I/Os into BST pins when a rising edge on TCK is detected while TMS is at logical low. Once the BST pins are in test mode they will remain in BST mode until the internal BST state machine reaches the "logic reset" state. At this point the BST pins will be released and will function as regular I/O pins. The "logic reset" state is reached 5 TCK cycles after the TMS pin is set to logical HIGH.

The Program fuse determines whether the device is in Dedicated Test or Flexible mode. The default (fuse not programmed) is Flexible mode.

Development Tool Support

The eX devices are fully supported by Actel's line of FPGA development tools, including the Actel DeskTOP series and Designer tools. The Actel DeskTOP series is an integrated design environment for PCs that includes design entry, simulation, synthesis, and place-and-route tools. Designer,

Actel's suite of FPGA development point tools for PCs and Workstations, includes the ACTgen Macro Builder, timing driven place-and-route analysis tools, and fuse file generation.

In addition, the eX devices contain internal probe circuitry that provides built-in access to the output of every C-cell, R-cell, and routed clock in the design, enabling 100-percent real-time observation and analysis of a device's internal logic nodes without design iteration. The probe circuitry is accessed by Silicon Explorer II, an easy-to-use integrated verification and logic analysis tool that can sample data at 100 MHz (asynchronous) or 66 MHz (synchronous). Silicon Explorer II attaches to a PC's standard COM port, turning the PC into a fully functional 18-channel logic analyzer. Silicon Explorer II allows designers to complete the design verification process at their desks and reduces verification time from several hours per cycle to only a few seconds.

eX Probe Circuit Control Pins

The Silicon Explorer II tool uses the boundary scan ports (TDI, TCK, TMS and TDO) to select the desired nets for verification. The selected internal nets are assigned to the PRA/PRB pins for observation. Figure 7 illustrates the interconnection between Silicon Explorer II and the FPGA to perform in-circuit verification. The TRST pin is equipped with an internal pull-up resistor. To remove the boundary scan state machine from the reset state during probing, it is recommended that the TRST pin be left floating.

Design Considerations

For prototyping, the TDI, TCK, TDO, PRA, and PRB pins should not be used as input or bidirectional ports. Because these pins are active during probing, critical signals input through these pins are not available while probing. In addition, the Security Fuse should not be programmed because doing so disables the probe circuitry.

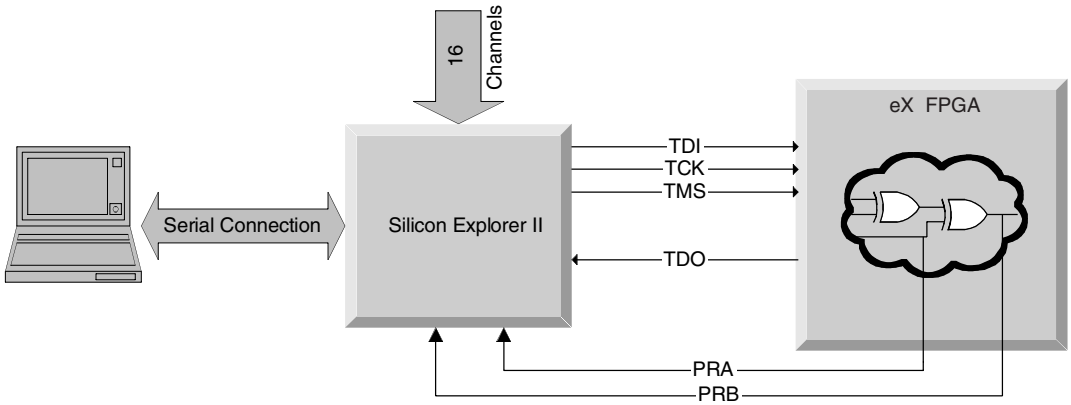


Figure 7 • *Probe Setup*

2.5V/3.3V/5.0V Operating Conditions

Absolute Maximum Ratings[1]

Symbol	Parameter	Limits	Units
V_{CCI}	DC Supply Voltage	–0.3 to +6.0	V
V_{CCA}	DC Supply Voltage	–0.3 to +3.0	V
V_I	Input Voltage	–0.5 to +5.5	V
V_O	Output Voltage	–0.5 to +V_{CCI} + 0.5	V
T_{STG}	Storage Temperature	–65 to +150	°C

Note:

1. *Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. Devices should not be operated outside the Recommended Operating Conditions.*

Recommended Operating Conditions

Parameter	Commercial	Industrial	Units
Temperature Range[1]	0 to +70	–40 to +85	°C
2.5V Power Supply Tolerance	±8	±8	%V_{CC}
3.3V Power Supply Tolerance	±9	±9	%V_{CC}
5.0V Power Supply Tolerance	±5	±10	%V_{CC}

Note:

1. *Ambient temperature (T_A).*

2.5V Electrical Specifications

Symbol	Parameter		Commercial Min.	Commercial Max.	Commercial '–F' Min.	Commercial '–F' Max.	Industrial Min.	Industrial Max.	Units
V_{OH}	V_{DD} = MIN, V_I = V_{IH} or V_{IL}	(I_{OH} = -100µA)	2.1				2.1		V
	V_{DD} = MIN, V_I = V_{IH} or V_{IL}	(I_{OH} = -1 mA)	2.0				2.0		V
	V_{DD} = MIN, V_I = V_{IH} or V_{IL}	(I_{OH} = -2 mA)	1.7				1.7		V
V_{OL}	V_{DD} = MIN, V_I = V_{IH} or V_{IL}	(I_{OL}= 100µA)		0.2				0.2	V
	V_{DD} = MIN, V_I = V_{IH} or V_{IL}	(I_{OL}= 1mA)		0.4				0.4	V
	V_{DD} = MIN, V_I = V_{IH} or V_{IL}	(I_{OL}= 2 mA)		0.7				0.7	V
V_{IL}	Input Low Voltage, $V_{OUT} \le V_{VOL(max)}$		-0.3	0.7			-0.3	0.7	V
V_{IH}	Input High Voltage, $V_{OUT} \ge V_{VOH(min)}$		1.7	V_{DD} + 0.3			1.7	V_{DD} + 0.3	V
I_{OZ}	3-State Output Leakage Current, V_{OUT} = V_{CCI} or GND		–10	10			–10	10	µA
t_R, t_F[1,2]	Input Transition Time t_R, t_F			10				10	ns
C_{IO}	I/O Capacitance			10				10	pF
I_{CC}[3]	Standby Current			2.0		10		3.0	mA
IV Curve[4]	Can be derived from the IBIS model on the web.								

Notes:

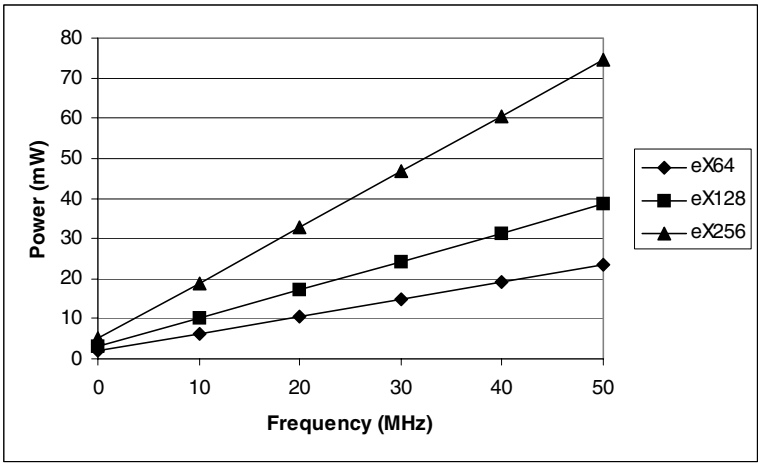
1. *t_R is the transition time from 0.7 V to 1.7V.*
2. *t_F is the transition time from 1.7V to 0.7V.*
3. *Individual device data is available in the www.actel.com/guru.*
4. *The IBIS model can be found at www.actel.com/support/support/support_ibis.html.*

2.5V Low Power Specifications
(Worst-Case Commercial Conditions, V_{CCA},V_{CCI} = 2.7V, T_J = 25°C)

Product	Low Power Standby Current	Units
eX64	175	µA
eX128	225	µA
eX256	250	µA

Note:

1. The power up/down resistors should not be used for low power designs.

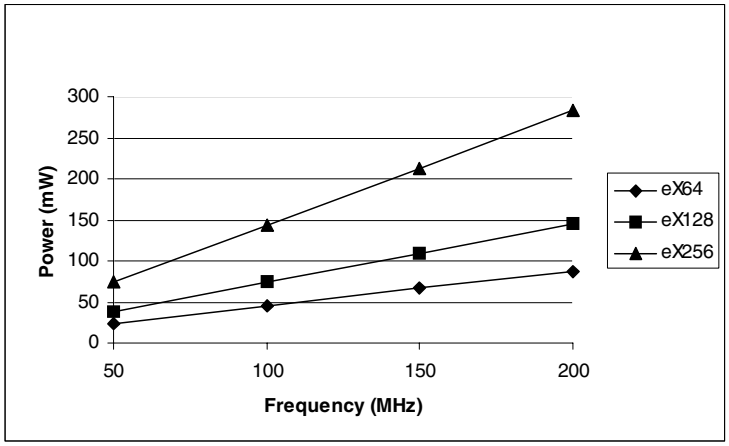


Notes:

1. Device filled with 16-bit counters.

2. V_{CCA}, V_{CCI} = 2.7V, device tested at room temperature.

Figure 8 • eX Dynamic Power Consumption – Low Frequency



Notes:

1. Device filled with 16-bit counters.

2. V_{CCA}, V_{CCI} = 2.7V, device tested at room temperature.

Figure 9 • eX Dynamic Power Consumption – High Frequency

3.3V and 5.0V Electrical Specifications

Symbol	Parameter		Commercial Min.	Commercial Max.	Commercial '–F' Min.	Commercial '–F' Max.	Industrial Min.	Industrial Max.	Units
V_{OH}	V_{DD} = MIN, $V_I = V_{IH}$ or V_{IL}	(I_{OH} = -1mA)	0.9 V_{CCI}				0.9 V_{CCI}		V
	V_{DD} = MIN, $V_I = V_{IH}$ or V_{IL}	(I_{OH} = -8mA)	2.4				2.4		V
V_{OL}	V_{DD} = MIN, $V_I = V_{IH}$ or V_{IL}	(I_{OL}= 1mA)		0.1 V_{CCI}				0.1 V_{CCI}	V
	V_{DD} = MIN, $V_I = V_{IH}$ or V_{IL}	(I_{OL}= 12mA)		0.4				0.4	V
V_{IL}	Input Low Voltage			0.8				0.8	V
V_{IH}	Input High Voltage		2.0				2.0		V
I_{IL}/ I_{IH}	Input Leakage Current, V_{IN} = V_{CCI} or GND		–10	10			–10	10	µA
I_{OZ}	3-State Output Leakage Current, V_{OUT} = V_{CCI} or GND		–10	10			–10	10	µA
t_R, t_F[1,2]	Input Transition Time t_R, t_F			10				10	ns
C_{IO}	I/O Capacitance			10				10	pF
I_{CC}[3]	Standby Current			4.0		10		10	mA
IV Curve[4]	Can be derived from the IBIS model on the web.								

Notes:

1. *t_R is the transition time from 0.8 V to 2.0V.*
2. *t_F is the transition time from 2.0V to 0.8V.*
3. *Individual device data is available in the www.actel.com/guru.*
4. *The IBIS model can be found at www.actel.com/support/support/support_ibis.html.*

Junction Temperature (T_J)

The temperature variable in the Designer Series software refers to the junction temperature, not the ambient temperature. This is an important distinction because the heat generated from dynamic power consumption is usually hotter than the ambient temperature. Equation 1, shown below, can be used to calculate junction temperature.

$$\text{Junction Temperature} = \Delta T + T_a \quad (1)$$

Where:

T_a = Ambient Temperature

ΔT = Temperature gradient between junction (silicon) and ambient

$\Delta T = \theta_{ja} * P$

P = Power

θ_{ja} = Junction to ambient of package. θ_{ja} numbers are located in the Package Thermal Characteristics section below.

Package Thermal Characteristics

The device junction to case thermal characteristic is θ_{jc}, and the junction to ambient air characteristic is θ_{ja}. The thermal characteristics for θ_{ja} are shown with two different air flow rates.

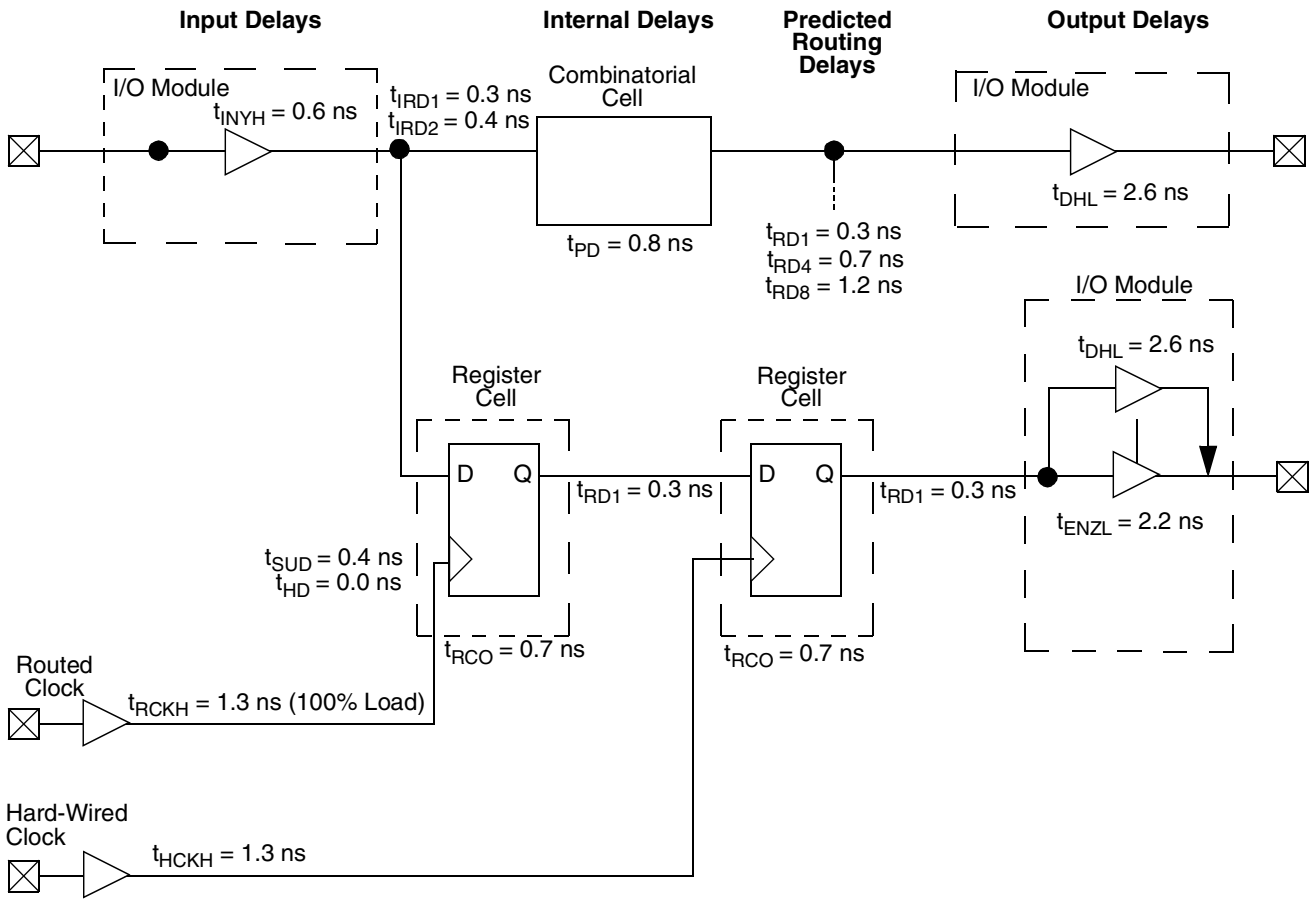
The maximum junction temperature is 150°C.

A sample calculation of the absolute maximum power dissipation allowed for a TQFP 100-pin package at commercial temperature and still air is as follows:

$$\text{Maximum Power Allowed} = \frac{\text{Max. junction temp. (°C)} - \text{Max. ambient temp. (°C)}}{\theta_{ja}(\text{°C/W})} = \frac{150\text{°C} - 70\text{°C}}{37.5\text{°C/W}} = 2.1\text{W}$$

Package Type	Pin Count	θ_{jc}	θ_{ja} Still Air	θ_{ja} 300 ft/min	Units
Thin Quad Flat Pack (TQFP)	64	14	51.2	35	°C/W
Thin Quad Flat Pack (TQFP)	100	12	37.5	30	°C/W
Chip Scale Package (CSP)	49	3	70.2	55.8	°C/W
Chip Scale Package (CSP)	128	3	54.1	47.8	°C/W
Chip Scale Package (CSP)	180	3	57.8	51	°C/W

eX Timing Model*



**Values shown for eX128–P, worst-case commercial conditions (5.0V, 35pF Pad load).*

Hard-Wired Clock

External Setup = $t_{INYH} + t_{IRD1} + t_{SUD} - t_{HCKL}$
= 0.6 + 0.3 + 0.4 – 1.3 = 0.0 ns

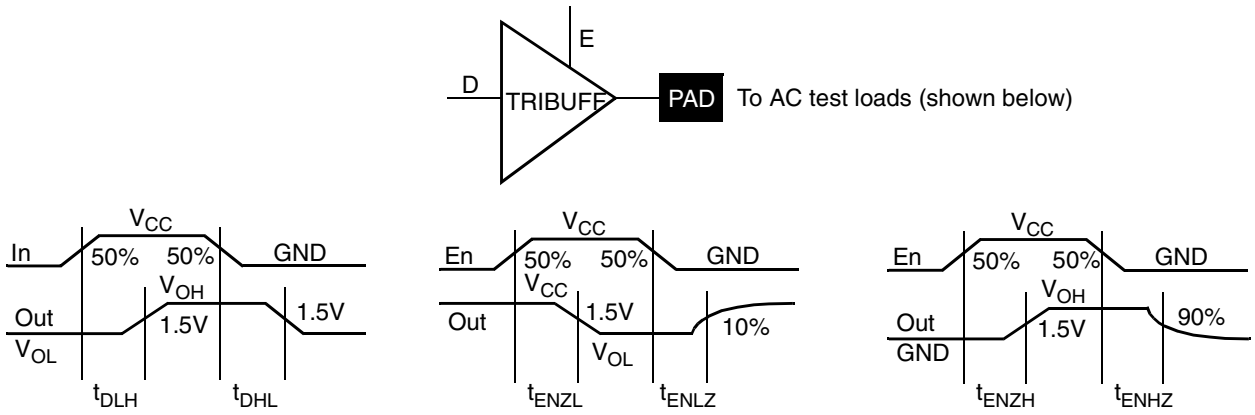
Clock-to-Out (Pad-to-Pad), typical
= $t_{HCKL} + t_{RCO} + t_{RD1} + t_{DLH}$
= 1.3 + 0.7 + 0.3 + 2.6 = 4.9 ns

Routed Clock

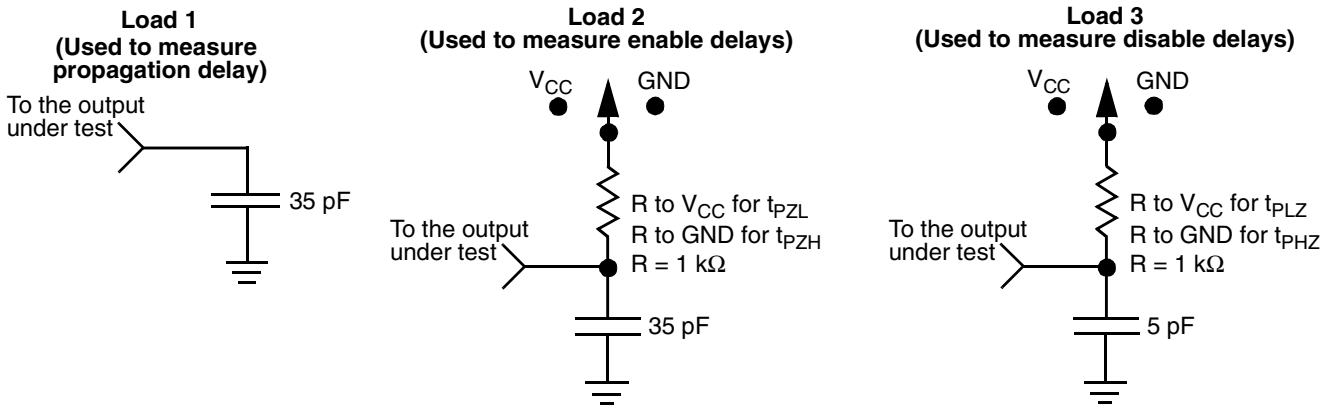
External Setup = $t_{INYH} + t_{IRD1} + t_{SUD} - t_{RCKH}$
= 0.6 + 0.3 + 0.4 – 1.3= 0.0 ns

Clock-to-Out (Pad-to-Pad), typical
= $t_{RCKH} + t_{RCO} + t_{RD1} + t_{DLH}$
= 1.3+ 0.7 + 0.3 + 2.6 = 4.9 ns

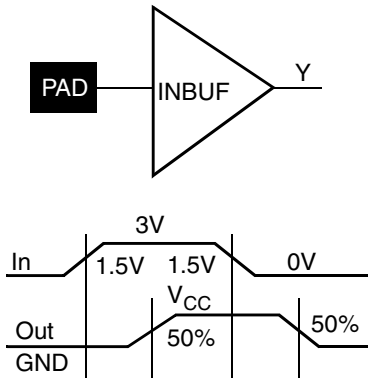
Output Buffer Delays



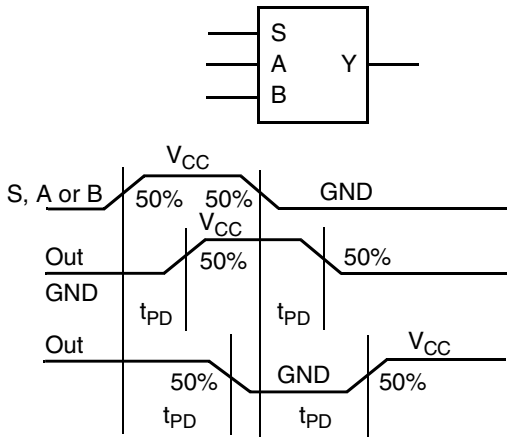
AC Test Loads



Input Buffer Delays

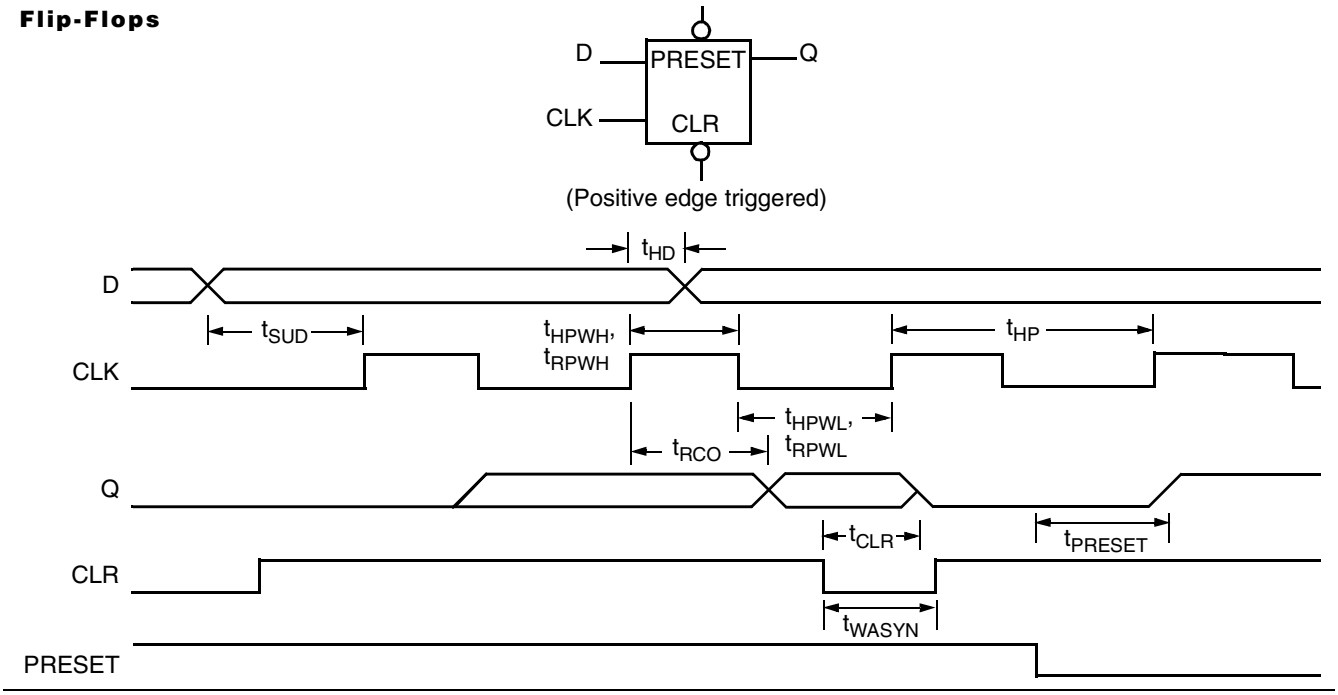


C-Cell Delays



Cell Timing Characteristics

Flip-Flops



Timing Characteristics

Timing characteristics for eX devices fall into three categories: family-dependent, device-dependent, and design-dependent. The input and output buffer characteristics are common to all eX family members. Internal routing delays are device-dependent. Design dependency means actual delays are not determined until after placement and routing of the user's design are complete. Delay values may then be determined by using the Timer utility or performing simulation with post-layout delays.

Critical Nets and Typical Nets

Propagation delays are expressed only for typical nets, which are used for initial design performance evaluation. Critical net delays can then be applied to the most timing critical paths. Critical nets are determined by net property assignment prior to placement and routing. Up to 6 percent of the nets in a design may be designated as critical, while 90 percent of the nets in a design are typical

Long Tracks

Some nets in the design use long tracks. Long tracks are special routing resources that span multiple rows, columns, or modules. Long tracks employ three to five antifuse connections. This increases capacitance and resistance, resulting in longer net delays for macros connected to long tracks. Typically, up to 6 percent of nets in a fully utilized device require long tracks. Long tracks contribute approximately 4 ns to 8.4 ns delay. This additional delay is represented statistically in higher fanout routing delays.

Timing Derating

eX devices are manufactured with a CMOS process. Therefore, device performance varies according to temperature, voltage, and process changes. Minimum timing parameters reflect maximum operating voltage, minimum operating temperature, and best-case processing. Maximum timing parameters reflect minimum operating voltage, maximum operating temperature, and worst-case processing.

Temperature and Voltage Derating Factors

(Normalized to Worst-Case Commercial, T_J = 70°C, V_{CCA} = 2.3V)

	Junction Temperature (T_J)						
V_{CCA}	–55	–40	0	25	70	85	125
2.3	0.75	0.79	0.88	0.89	1.00	1.04	1.16
2.5	0.70	0.74	0.82	0.83	0.93	0.97	1.08
2.7	0.66	0.69	0.79	0.79	0.88	0.92	1.02

eX Family Timing Characteristics

(Worst-Case Commercial Conditions, V_{CCA} = 2.3V, T_J = 70°C)

		'–P' Speed		'Std' Speed		'–F' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
C-Cell Propagation Delays[1]								
t_{PD}	Internal Array Module		0.8		1.2		1.7	ns
Predicted Routing Delays[2]								
t_{DC}	FO=1 Routing Delay, Direct Connect		0.1		0.1		0.2	ns
t_{FC}	FO=1 Routing Delay, Fast Connect		0.3		0.5		0.7	ns
t_{RD1}	FO=1 Routing Delay		0.3		0.5		0.7	ns
t_{RD2}	FO=2 Routing Delay		0.4		0.6		0.8	ns
t_{RD3}	FO=3 Routing Delay		0.5		0.8		1.1	ns
t_{RD4}	FO=4 Routing Delay		0.7		1.0		1.3	ns
t_{RD8}	FO=8 Routing Delay		1.2		1.7		2.4	ns
t_{RD12}	FO=12 Routing Delay		1.7		2.5		3.5	ns
R-Cell Timing								
t_{RCO}	Sequential Clock-to-Q		0.7		1.0		1.4	ns
t_{CLR}	Asynchronous Clear-to-Q		0.6		0.8		1.2	ns
t_{PRESET}	Asynchronous Preset-to-Q		0.7		0.9		1.3	ns
t_{SUD}	Flip-Flop Data Input Set-Up	0.4		0.6		0.8		ns
t_{HD}	Flip-Flop Data Input Hold	0.0		0.0		0.0		ns
t_{WASYN}	Asynchronous Pulse Width	1.3		1.9		2.6		ns
$t_{RECASYN}$	Asynchronous Recovery Time	0.3		0.5		0.7		ns
t_{HASYN}	Asynchronous Hold Time	0.3		0.5		0.7		ns
2.5V Input Module Propagation Delays								
t_{INYH}	Input Data Pad-to-Y HIGH		0.6		0.7		1.0	ns
t_{INYL}	Input Data Pad-to-Y LOW		0.8		1.0		1.5	ns
3.3V Input Module Propagation Delays								
t_{INYH}	Input Data Pad-to-Y HIGH		0.7		0.9		1.3	ns
t_{INYL}	Input Data Pad-to-Y LOW		1.0		1.3		1.9	ns
5.0V Input Module Propagation Delays								
t_{INYH}	Input Data Pad-to-Y HIGH		0.6		0.9		1.2	ns
t_{INYL}	Input Data Pad-to-Y LOW		0.8		1.1		1.5	ns
Input Module Predicted Routing Delays[2]								
t_{IRD1}	FO=1 Routing Delay		0.3		0.4		0.5	ns
t_{IRD2}	FO=2 Routing Delay		0.4		0.6		0.8	ns
t_{IRD3}	FO=3 Routing Delay		0.5		0.8		1.1	ns
t_{IRD4}	FO=4 Routing Delay		0.7		1.0		1.3	ns
t_{IRD8}	FO=8 Routing Delay		1.2		1.7		2.4	ns
t_{IRD12}	FO=12 Routing Delay		1.7		2.5		3.5	ns

Notes:

1. *For dual-module macros, use $t_{PD} + t_{RD1} + t_{PDw}$ $t_{RCO} + t_{RD1} + t_{PDn}$ or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.*
2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance.*

eX Family Timing Characteristics (Continued)

(Worst-Case Commercial Conditions V_{CCA} = 2.3V, V_{CCI} = 4.75V, T_J = 70°C)

		'–P' Speed		'Std' Speed		'–F' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
Dedicated (Hard-Wired) Array Clock Networks								
t_{HCKH}	Input LOW to HIGH (Pad to R-Cell Input)		1.3		1.7		2.6	ns
t_{HCKL}	Input HIGH to LOW (Pad to R-Cell Input)		1.1		1.5		2.2	ns
t_{HPWH}	Minimum Pulse Width HIGH	1.5		2.1		3.0		ns
t_{HPWL}	Minimum Pulse Width LOW	1.5		2.1		3.0		ns
t_{HCKSW}	Maximum Skew		<0.1		<0.1		<0.1	ns
t_{HP}	Minimum Period	3.0		4.2		6.0		ns
f_{HMAX}	Maximum Frequency		333		238		167	MHz
Routed Array Clock Networks								
t_{RCKH}	Input LOW to HIGH (Light Load) (Pad to R-Cell Input) MAX.		1.1		1.6		2.2	ns
t_{RCKL}	Input HIGH to LOW (Light Load) (Pad to R-Cell Input) MAX.		1.4		1.9		2.7	ns
t_{RCKH}	Input LOW to HIGH (50% Load) (Pad to R-Cell Input) MAX.		1.2		1.7		2.4	ns
t_{RCKL}	Input HIGH to LOW (50% Load) (Pad to R-Cell Input) MAX.		1.4		1.9		2.7	ns
t_{RCKH}	Input LOW to HIGH (100% Load) (Pad to R-Cell Input) MAX.		1.3		1.9		2.6	ns
t_{RCKL}	Input HIGH to LOW (100% Load) (Pad to R-Cell Input) MAX.		1.5		2.0		2.9	ns
t_{RPWH}	Min. Pulse Width HIGH	1.5		2.1		3.0		ns
t_{RPWL}	Min. Pulse Width LOW	1.5		2.1		3.0		ns
t_{RCKSW}[1]	Maximum Skew (Light Load)		0.2		0.3		0.4	ns
t_{RCKSW}[1]	Maximum Skew (50% Load)		0.1		0.2		0.3	ns
t_{RCKSW}[1]	Maximum Skew (100% Load)		0.1		0.1		0.2	ns

Note:

1. Clock skew improves as the clock network becomes more heavily loaded.

eX Family Timing Characteristics (Continued)

(Worst-Case Commercial Conditions V_{CCA} = 2.3V, V_{CCI} = 2.3V or 3.0V, T_J = 70°C)

		‘–P’ Speed		‘Std’ Speed		‘–F’ Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
Dedicated (Hard-Wired) Array Clock Networks								
t_{HCKH}	Input LOW to HIGH (Pad to R-Cell Input)		1.3		1.8		2.7	ns
t_{HCKL}	Input HIGH to LOW (Pad to R-Cell Input)		1.2		1.5		2.3	ns
t_{HPWH}	Minimum Pulse Width HIGH	1.5		2.1		3.0		ns
t_{HPWL}	Minimum Pulse Width LOW	1.5		2.1		3.0		ns
t_{HCKSW}	Maximum Skew		<0.1		<0.1		<0.1	ns
t_{HP}	Minimum Period	3.0		4.2		6.0		ns
f_{HMAX}	Maximum Frequency		333		238		167	MHz
Routed Array Clock Networks								
t_{RCKH}	Input LOW to HIGH (Light Load) (Pad to R-Cell Input) MAX.		1.0		1.4		2.0	ns
t_{RCKL}	Input HIGH to LOW (Light Load) (Pad to R-Cell Input) MAX.		1.5		2.1		2.9	ns
t_{RCKH}	Input LOW to HIGH (50% Load) (Pad to R-Cell Input) MAX.		1.2		1.7		2.4	ns
t_{RCKL}	Input HIGH to LOW (50% Load) (Pad to R-Cell Input) MAX.		1.5		2.1		3.0	ns
t_{RCKH}	Input LOW to HIGH (100% Load) (Pad to R-Cell Input) MAX.		1.4		2.0		2.8	ns
t_{RCKL}	Input HIGH to LOW (100% Load) (Pad to R-Cell Input) MAX.		1.6		2.2		3.1	ns
t_{RPWH}	Min. Pulse Width HIGH	1.5		2.1		3.0		ns
t_{RPWL}	Min. Pulse Width LOW	1.5		2.1		3.0		ns
t_{RCKSW}[1]	Maximum Skew (Light Load)		0.2		0.3		0.4	ns
t_{RCKSW}[1]	Maximum Skew (50% Load)		0.2		0.2		0.3	ns
t_{RCKSW}[1]	Maximum Skew (100% Load)		0.1		0.1		0.2	ns

Note:

1. Clock skew improves as the clock network becomes more heavily loaded.

eX Family Timing Characteristics (Continued)

(Worst-Case Commercial Conditions V_{CCA} = 2.3V, T_J = 70°C)

		'–P' Speed		'Std' Speed		'–F' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
2.5V LVTTL Output Module Timing[1] (V_{CCI} = 2.3V)								
t_{DLH}	Data-to-Pad LOW to HIGH		3.4		4.9		6.9	ns
t_{DHL}	Data-to-Pad HIGH to LOW		3.6		5.14		7.20	ns
t_{DHLS}	Data-to-Pad HIGH to LOW—Low Slew		11.9		17.0		23.8	ns
t_{ENZL}	Enable-to-Pad, Z to L		2.5		3.6		5.1	ns
t_{ENZLS}	Enable-to-Pad Z to L—Low Slew		11.8		16.9		23.7	ns
t_{ENZH}	Enable-to-Pad, Z to H		3.4		4.9		6.9	ns
t_{ENLZ}	Enable-to-Pad, L to Z		2.1		3.0		4.2	ns
t_{ENHZ}	Enable-to-Pad, H to Z		2.4		5.67		7.94	ns
d_{TLH}	Delta LOW to HIGH		0.034		0.046		0.066	ns/pF
d_{THL}	Delta HIGH to LOW		0.016		0.022		0.05	ns/pF
d_{THLS}	Delta HIGH to LOW—Low Slew		0.05		0.072		0.1	ns/pF
3.3V LVTTL Output Module Timing[1] (V_{CCI} = 3.0V)								
t_{DLH}	Data-to-Pad LOW to HIGH		2.8		4.0		5.6	ns
t_{DHL}	Data-to-Pad HIGH to LOW		2.7		3.9		5.4	ns
t_{DHLS}	Data-to-Pad HIGH to LOW—Low Slew		9.8		14		19.7	ns
t_{ENZL}	Enable-to-Pad, Z to L		2.2		3.2		4.4	ns
t_{ENZLS}	Enable-to-Pad Z to L—Low Slew		9.7		13.9		19.6	ns
t_{ENZH}	Enable-to-Pad, Z to H		2.8		4.0		5.6	ns
t_{ENLZ}	Enable-to-Pad, L to Z		2.8		4.0		5.6	ns
t_{ENHZ}	Enable-to-Pad, H to Z		2.6		3.8		5.3	ns
d_{TLH}	Delta LOW to HIGH		0.02		0.03		0.046	ns/pF
d_{THL}	Delta HIGH to LOW		0.016		0.022		0.05	ns/pF
d_{THLS}	Delta HIGH to LOW—Low Slew		0.05		0.072		0.1	ns/pF
5.0V TTL Output Module Timing[1] (V_{CCI} = 4.75V)								
t_{DLH}	Data-to-Pad LOW to HIGH		2.0		2.9		4.0	ns
t_{DHL}	Data-to-Pad HIGH to LOW		2.6		3.7		5.2	ns
t_{DHLS}	Data-to-Pad HIGH to LOW—Low Slew		6.9		9.9		13.8	ns
t_{ENZL}	Enable-to-Pad, Z to L		1.9		2.7		3.8	ns
t_{ENZLS}	Enable-to-Pad Z to L—Low Slew		6.8		9.8		13.7	ns
t_{ENZH}	Enable-to-Pad, Z to H		2.1		3.0		4.1	ns
t_{ENLZ}	Enable-to-Pad, L to Z		3.3		4.8		6.6	ns
t_{ENHZ}	Enable-to-Pad, H to Z		2.7		3.8		5.3	ns
d_{TLH}	Delta LOW to HIGH		0.014		0.024		0.035	ns/pF
d_{THL}	Delta HIGH to LOW		0.014		0.024		0.035	ns/pF
d_{THLS}	Delta HIGH to LOW—Low Slew		0.042		0.06		0.082	ns/pF

Note:

1. Delays based on 35 pF loading.

Pin Description

CLKA/B Clock A and B

These pins are clock inputs for clock distribution networks. Input levels are compatible with standard TTL or LVTTL specifications. The clock input is buffered prior to clocking the R-cells. If not used, this pin must be set LOW or HIGH on the board. It must not be left floating.

GND Ground

LOW supply voltage.

HCLK Dedicated (Hard-wired) Array Clock

This pin is the clock input for sequential modules. Input levels are compatible with standard TTL or LVTTL specifications. This input is directly wired to each R-cell and offers clock speeds independent of the number of R-cells being driven. If not used, this pin must be set LOW or HIGH on the board. It must not be left floating.

I/O Input/Output

The I/O pin functions as an input, output, tristate, or bidirectional buffer. Based on certain configurations, input and output levels are compatible with standard TTL or LVTTL specifications. Unused I/O pins are automatically tristated by the Designer Series software.

NC No Connection

This pin is not connected to circuitry within the device. These pins can be driven to any voltage or can be left floating with no effect on the operation of the device.

PRA, I/O
PRB, I/O Probe A/B

The Probe pin is used to output data from any user-defined design node within the device. This independent diagnostic pin can be used in conjunction with the other probe pin to allow real-time diagnostic output of any signal path within the device. The Probe pin can be used as a user-defined I/O when verification has been completed. The pin's probe capabilities can be permanently disabled to protect programmed design confidentiality.

TCK, I/O Test Clock

Test clock input for diagnostic probe and device programming. In flexible mode, TCK becomes active when the TMS pin is set LOW (refer to Table 3 on page 6). This pin functions as an I/O when the boundary scan state machine reaches the "logic reset" state.

TDI, I/O Test Data Input

Serial input for boundary scan testing and diagnostic probe. In flexible mode, TDI is active when the TMS pin is set LOW (refer to Table 3 on page 6). This pin functions as an I/O when the boundary scan state machine reaches the "logic reset" state.

TDO, I/O Test Data Output

Serial output for boundary scan testing. In flexible mode, TDO is active when the TMS pin is set LOW (refer to Table 3 on page 6). This pin functions as an I/O when the boundary scan state machine reaches the "logic reset" state.

TMS Test Mode Select

The TMS pin controls the use of the IEEE 1149.1 Boundary Scan pins (TCK, TDI, TDO, TRST). In flexible mode when the TMS pin is set LOW, the TCK, TDI, and TDO pins are boundary scan pins (refer to Table 3 on page 6). Once the boundary scan pins are in test mode, they will remain in that mode until the internal boundary scan state machine reaches the "logic reset" state. At this point, the boundary scan pins will be released and will function as regular I/O pins. The "logic reset" state is reached 5 TCK cycles after the TMS pin is set HIGH. In dedicated test mode, TMS functions as specified in the IEEE 1149.1 specifications.

TRST, I/O Boundary Scan Reset Pin

Once it is configured as the JTAG Reset pin, the TRST pin functions as an active-low input to asynchronously initialize or reset the boundary scan circuit. The TRST pin is equipped with an internal pull-up resistor. This pin functions as an I/O when the "Reserve JTAG Reset Pin" is not selected in Designer.

V_{CCI} Supply Voltage

Supply voltage for I/Os. See Table 2 on page 6.

V_{CCA} Supply Voltage

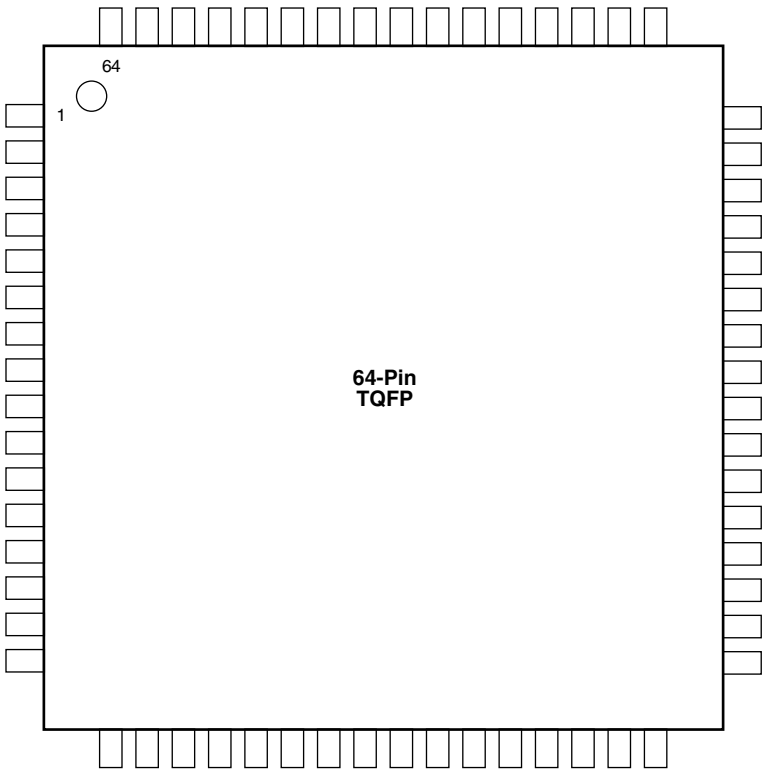
Supply voltage for Array. See Table 2 on page 6.

LP Low Power Pin

Controls the low power mode of the eX devices. The device is placed in the low power mode by connecting the LP pin to logic high. In low power mode, all I/Os are tristated, all input buffers are turned OFF, and the core of the devices is turned OFF. To exit the low power mode, the LP pin must be set LOW. The device enters the low power mode 800ns after the LP pin is driven to a logical high. It will resume normal operation in 200µs after the LP pin is driven to a logic low. The logic high level on the LP pin must never exceed V_{CCI}+ 0.5V.

Package Pin Assignments

64-Pin TQFP (Top View)



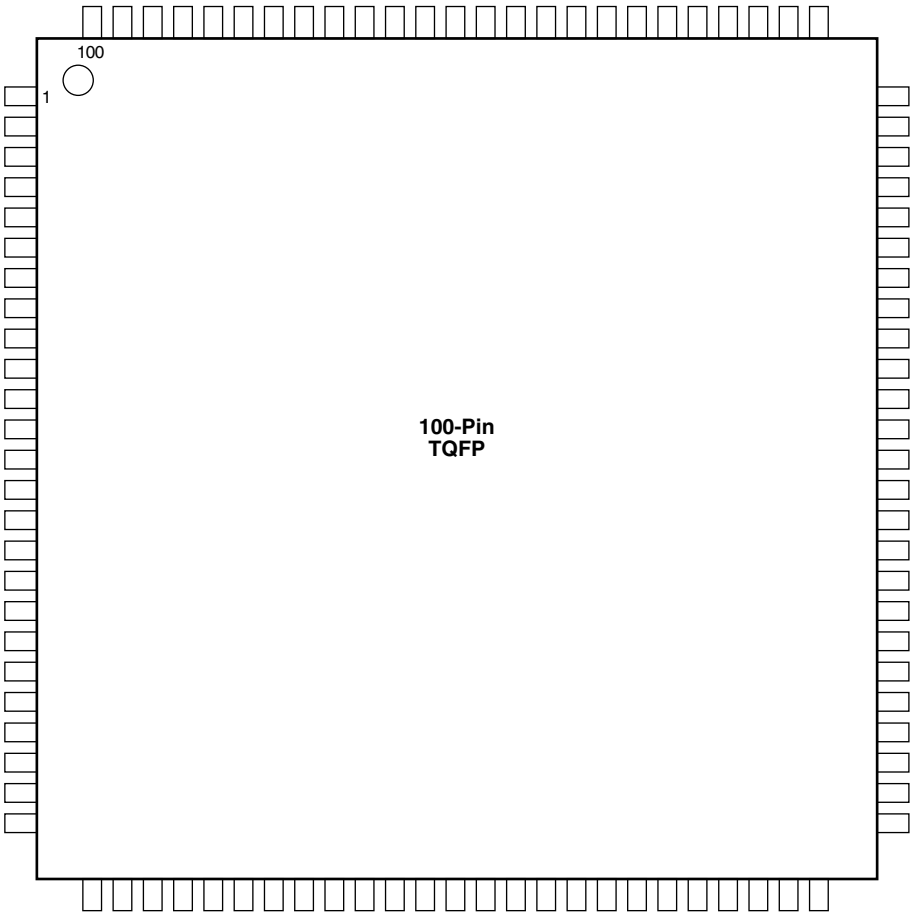
64-Pin TQFP

Pin Number	eX64 Function	eX128 Function
1	GND	GND
2	TDI, I/O	TDI, I/O
3	I/O	I/O
4	TMS	TMS
5	GND	GND
6	V_{CCI}	V_{CCI}
7	I/O	I/O
8	I/O	I/O
9	NC	I/O
10	NC	I/O
11	TRST, I/O	TRST, I/O
12	I/O	I/O
13	NC	I/O
14	GND	GND
15	I/O	I/O
16	I/O	I/O
17	I/O	I/O
18	I/O	I/O
19	V_{CCI}	V_{CCI}
20	I/O	I/O
21	PRB, I/O	PRB, I/O
22	V_{CCA}	V_{CCA}
23	GND	GND
24	I/O	I/O
25	HCLK	HCLK
26	I/O	I/O
27	I/O	I/O
28	I/O	I/O
29	I/O	I/O
30	I/O	I/O
31	I/O	I/O
32	TDO, I/O	TDO, I/O
33	GND	GND
34	I/O	I/O
35	I/O	I/O
36	V_{CCI}*	V_{CCI}*
37	V_{CCI}	V_{CCI}
38	I/O	I/O
39	I/O	I/O
40	NC	I/O
41	NC	I/O
42	I/O	I/O
43	I/O	I/O
44	V_{CCA}	V_{CCA}
45	LP, GND	LP, GND
46	GND	GND
47	I/O	I/O
48	I/O	I/O
49	I/O	I/O
50	I/O	I/O
51	I/O	I/O
52	V_{CCI}	V_{CCI}
53	I/O	I/O
54	I/O	I/O
55	CLKA	CLKA
56	CLKB	CLKB
57	V_{CCA}	V_{CCA}
58	GND	GND
59	PRA, I/O	PRA, I/O
60	I/O	I/O
61	V_{CCI}	V_{CCI}
62	I/O	I/O
63	I/O	I/O
64	TCK, I/O	TCK, I/O

Note: *This V_{CCI} pin may optionally be connected to V_{CCA} if the LP pin is not being used.*

Package Pin Assignments (Continued)

100-Pin TQFP (Top View)



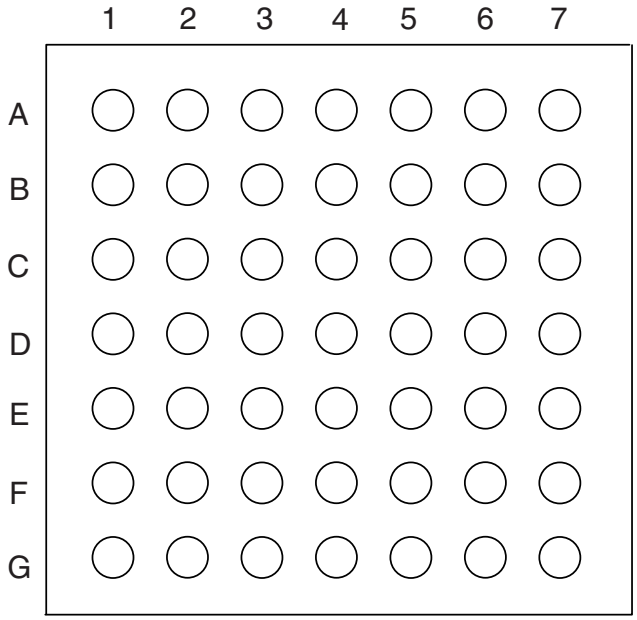
100-TQFP

Pin Number	eX64 Function	eX128 Function	eX256 Function
1	GND	GND	GND
2	TDI, I/O	TDI, I/O	TDI, I/O
3	NC	NC	I/O
4	NC	NC	I/O
5	NC	NC	I/O
6	I/O	I/O	I/O
7	TMS	TMS	TMS
8	V_{CCI}	V_{CCI}	V_{CCI}
9	GND	GND	GND
10	NC	I/O	I/O
11	NC	I/O	I/O
12	I/O	I/O	I/O
13	NC	I/O	I/O
14	I/O	I/O	I/O
15	NC	I/O	I/O
16	TRST, I/O	TRST, I/O	TRST, I/O
17	NC	I/O	I/O
18	I/O	I/O	I/O
19	NC	I/O	I/O
20	V_{CCI}	V_{CCI}	V_{CCI}
21	I/O	I/O	I/O
22	NC	I/O	I/O
23	NC	NC	I/O
24	NC	NC	I/O
25	I/O	I/O	I/O
26	I/O	I/O	I/O
27	I/O	I/O	I/O
28	I/O	I/O	I/O
29	I/O	I/O	I/O
30	I/O	I/O	I/O
31	I/O	I/O	I/O
32	I/O	I/O	I/O
33	I/O	I/O	I/O
34	PRB, I/O	PRB, I/O	PRB, I/O
35	V_{CCA}	V_{CCA}	V_{CCA}
36	GND	GND	GND
37	NC	NC	NC
38	I/O	I/O	I/O
39	HCLK	HCLK	HCLK
40	I/O	I/O	I/O
41	I/O	I/O	I/O
42	I/O	I/O	I/O
43	I/O	I/O	I/O
44	V_{CCI}	V_{CCI}	V_{CCI}
45	I/O	I/O	I/O
46	I/O	I/O	I/O
47	I/O	I/O	I/O
48	I/O	I/O	I/O
49	TDO, I/O	TDO, I/O	TDO, I/O
50	NC	I/O	I/O
51	GND	GND	GND
52	NC	NC	I/O
53	NC	NC	I/O
54	NC	NC	I/O
55	I/O	I/O	I/O
56	I/O	I/O	I/O
57	V_{CCI}*	V_{CCI}*	V_{CCI}*
58	V_{CCI}	V_{CCI}	V_{CCI}
59	NC	I/O	I/O
60	I/O	I/O	I/O
61	NC	I/O	I/O
62	I/O	I/O	I/O
63	NC	I/O	I/O
64	I/O	I/O	I/O
65	NC	I/O	I/O
66	I/O	I/O	I/O
67	V_{CCA}	V_{CCA}	V_{CCA}
68	GND, LP	GND, LP	GND, LP
69	GND	GND	GND
70	I/O	I/O	I/O
71	I/O	I/O	I/O
72	NC	I/O	I/O
73	NC	NC	I/O
74	NC	NC	I/O
75	NC	NC	I/O
76	NC	I/O	I/O
77	I/O	I/O	I/O
78	I/O	I/O	I/O
79	I/O	I/O	I/O
80	I/O	I/O	I/O
81	I/O	I/O	I/O
82	V_{CCI}	V_{CCI}	V_{CCI}
83	I/O	I/O	I/O
84	I/O	I/O	I/O
85	I/O	I/O	I/O
86	I/O	I/O	I/O
87	CLKA	CLKA	CLKA
88	CLKB	CLKB	CLKB
89	NC	NC	NC
90	V_{CCA}	V_{CCA}	V_{CCA}
91	GND	GND	GND
92	PRA, I/O	PRA, I/O	PRA, I/O
93	I/O	I/O	I/O
94	I/O	I/O	I/O
95	I/O	I/O	I/O
96	I/O	I/O	I/O
97	I/O	I/O	I/O
98	I/O	I/O	I/O
99	I/O	I/O	I/O
100	TCK, I/O	TCK, I/O	TCK, I/O

Note: *This V_{CCI} pin may optionally be connected to V_{CCA} if the LP pin is not being used.*

Package Pin Assignments (Continued)

49-Pin CSP (Top View)



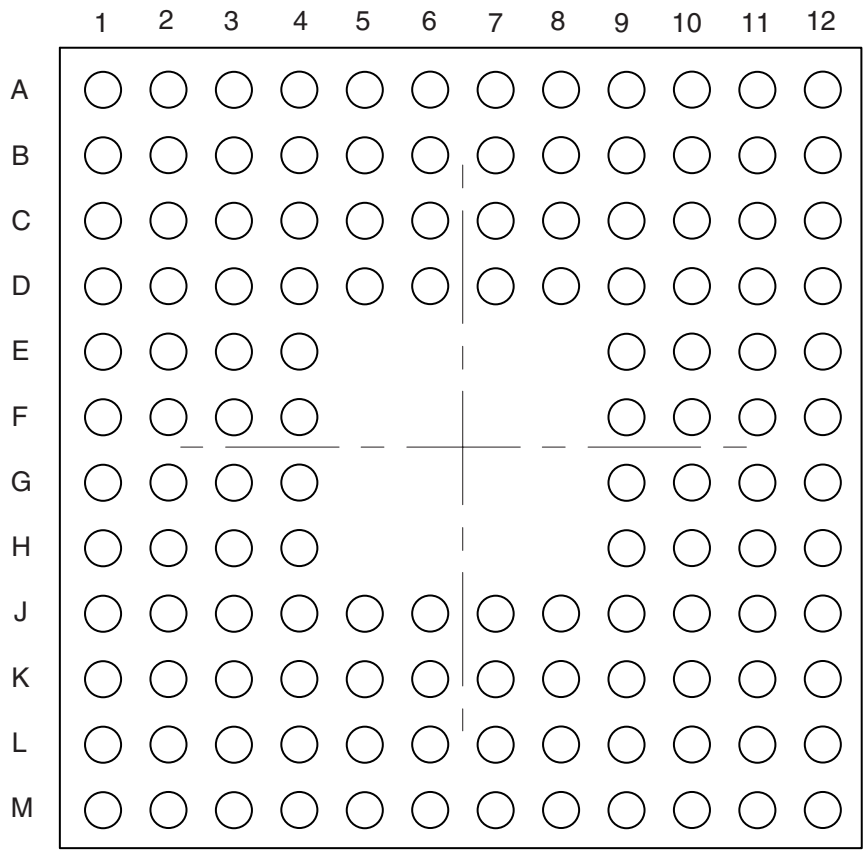
49-Pin CSP

Pin Number	eX64 Function	eX128 Function
A1	I/O	I/O
A2	I/O	I/O
A3	I/O	I/O
A4	I/O	I/O
A5	V_{CCA}	V_{CCA}
A6	I/O	I/O
A7	I/O	I/O
B1	TCK, I/O	TCK, I/O
B2	I/O	I/O
B3	I/O	I/O
B4	PRA, I/O	PRA, I/O
B5	CLKA	CLKA
B6	I/O	I/O
B7	GND, LP	GND, LP
C1	I/O	I/O
C2	TDI, I/O	TDI, I/O
C3	V_{CCI}	V_{CCI}
C4	GND	GND
C5	CLKB	CLKB
C6	V_{CCA}	V_{CCA}
C7	I/O	I/O
D1	I/O	I/O
D2	TMS	TMS
D3	GND	GND
D4	GND	GND
D5	V_{CCI}*	V_{CCI}*
D6	I/O	I/O
D7	I/O	I/O
E1	I/O	I/O
E2	TRST, I/O	TRST, I/O
E3	V_{CCI}	V_{CCI}
E4	GND	GND
E5	I/O	I/O
E6	I/O	I/O
E7	V_{CCI}	V_{CCI}
F1	I/O	I/O
F2	I/O	I/O
F3	I/O	I/O
F4	I/O	I/O
F5	HCLK	HCLK
F6	I/O	I/O
F7	TDO, I/O	TDO, I/O
G1	I/O	I/O
G2	I/O	I/O
G3	I/O	I/O
G4	PRB, I/O	PRB, I/O
G5	V_{CCA}	V_{CCA}
G6	I/O	I/O
G7	I/O	I/O

Note: *This V_{CCI} pin may optionally be connected to V_{CCA} if the LP pin is not being used.*

Package Pin Assignments (Continued)

128-Pin CSP (Top View)



128-CSP

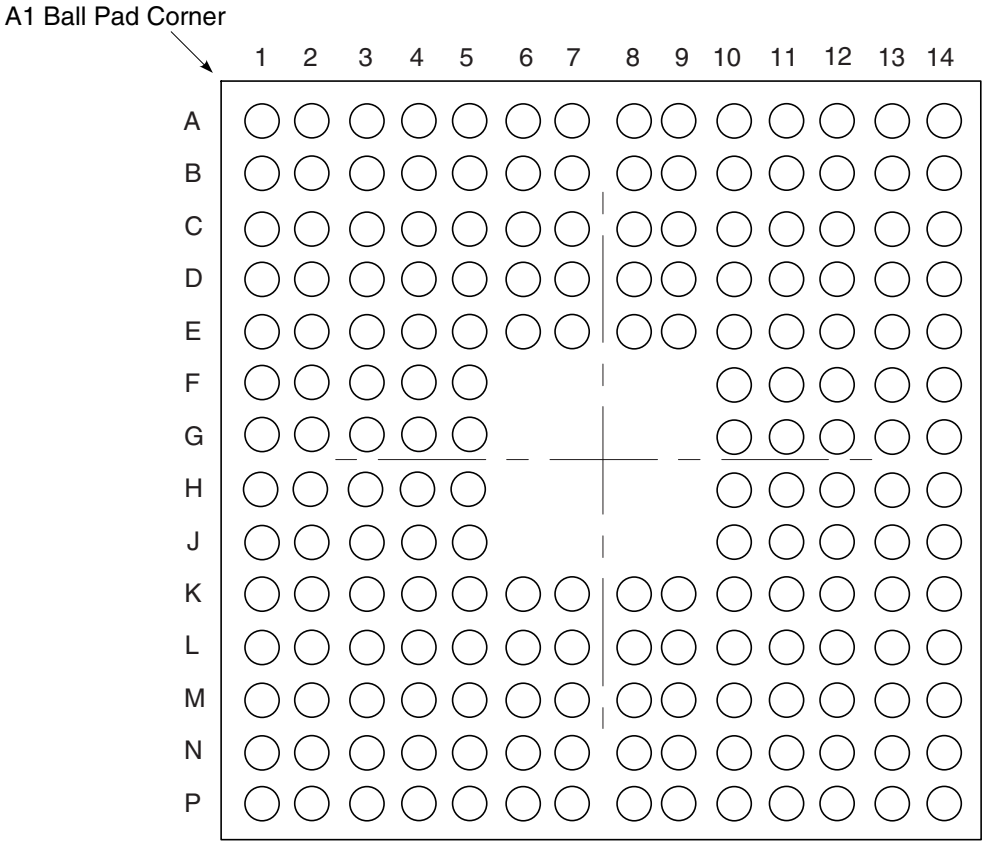
Pin Number	eX64 Function	eX128 Function	eX256 Function
A1	I/O	I/O	I/O
A2	TCK, I/O	TCK, I/O	TCK, I/O
A3	V_{CCI}	V_{CCI}	V_{CCI}
A4	I/O	I/O	I/O
A5	I/O	I/O	I/O
A6	V_{CCA}	V_{CCA}	V_{CCA}
A7	I/O	I/O	I/O
A8	I/O	I/O	I/O
A9	V_{CCI}	V_{CCI}	V_{CCI}
A10	I/O	I/O	I/O
A11	I/O	I/O	I/O
A12	I/O	I/O	I/O
B1	TMS	TMS	TMS
B2	I/O	I/O	I/O
B3	I/O	I/O	I/O
B4	I/O	I/O	I/O
B5	I/O	I/O	I/O
B6	PRA, I/O	PRA, I/O	PRA, I/O
B7	CLKB	CLKB	CLKB
B8	I/O	I/O	I/O
B9	I/O	I/O	I/O
B10	I/O	I/O	I/O
B11	GND	GND	GND
B12	I/O	I/O	I/O
C1	I/O	I/O	I/O
C2	TDI, I/O	TDI, I/O	TDI, I/O
C3	I/O	I/O	I/O
C4	I/O	I/O	I/O
C5	I/O	I/O	I/O
C6	CLKA	CLKA	CLKA
C7	I/O	I/O	I/O
C8	I/O	I/O	I/O
C9	I/O	I/O	I/O
C10	NC	I/O	I/O
C11	NC	I/O	I/O
C12	I/O	I/O	I/O
D1	NC	I/O	I/O
D2	I/O	I/O	I/O
D3	I/O	I/O	I/O
D4	I/O	I/O	I/O
D5	I/O	I/O	I/O
D6	GND	GND	GND
D7	I/O	I/O	I/O
D8	GND	GND	GND
D9	I/O	I/O	I/O
D10	I/O	I/O	I/O
D11	I/O	I/O	I/O
D12	V_{CCI}	V_{CCI}	V_{CCI}
E1	NC	I/O	I/O
E2	V_{CCI}	V_{CCI}	V_{CCI}
E3	I/O	I/O	I/O
E4	GND	GND	GND
E9	GND	GND	GND
E10	I/O	I/O	I/O
E11	GND, LP	GND, LP	GND, LP
E12	V_{CCA}	V_{CCA}	V_{CCA}
F1	NC	I/O	I/O
F2	NC	I/O	I/O
F3	NC	I/O	I/O
F4	I/O	I/O	I/O
F9	GND	GND	GND
F10	NC	I/O	I/O
F11	I/O	I/O	I/O
F12	I/O	I/O	I/O
G1	NC	I/O	I/O
G2	TRST, I/O	TRST, I/O	TRST, I/O
G3	I/O	I/O	I/O
G4	GND	GND	GND
G9	GND	GND	GND
G10	NC	I/O	I/O
G11	I/O	I/O	I/O
G12	NC	I/O	I/O
H1	GND	GND	GND
H2	I/O	I/O	I/O
H3	V_{CCI}	V_{CCI}	V_{CCI}
H4	GND	GND	GND
H9	I/O	I/O	I/O
H10	V_{CCI}	V_{CCI}	V_{CCI}

128-CSP

Pin Number	eX64 Function	eX128 Function	eX256 Function
H11	V_{CCI}*	V_{CCI}*	V_{CCI}*
H12	NC	I/O	I/O
J1	NC	NC	V_{CCI}*
J2	I/O	I/O	I/O
J3	V_{CCI}	V_{CCI}	V_{CCI}
J4	I/O	I/O	I/O
J5	I/O	I/O	I/O
J6	I/O	I/O	I/O
J7	GND	GND	GND
J8	I/O	I/O	I/O
J9	GND	GND	GND
J10	I/O	I/O	I/O
J11	I/O	I/O	I/O
J12	NC	I/O	I/O
K1	NC	I/O	I/O
K2	I/O	I/O	I/O
K3	I/O	I/O	I/O
K4	I/O	I/O	I/O
K5	I/O	I/O	I/O
K6	PRB, I/O	PRB, I/O	PRB, I/O
K7	HCLK	HCLK	HCLK
K8	I/O	I/O	I/O
K9	I/O	I/O	I/O
K10	I/O	I/O	I/O
K11	TDO, I/O	TDO, I/O	TDO, I/O
K12	I/O	I/O	I/O
L1	I/O	I/O	I/O
L2	I/O	I/O	I/O
L3	NC	I/O	I/O
L4	I/O	I/O	I/O
L5	I/O	I/O	I/O
L6	I/O	I/O	I/O
L7	I/O	I/O	I/O
L8	I/O	I/O	I/O
L9	I/O	I/O	I/O
L10	I/O	I/O	I/O
L11	NC	I/O	I/O
L12	V_{CCI}	V_{CCI}	V_{CCI}
M1	GND	GND	GND
M2	I/O	I/O	I/O
M3	I/O	I/O	I/O
M4	I/O	I/O	I/O
M5	I/O	I/O	I/O
M6	I/O	I/O	I/O
M7	V_{CCA}	V_{CCA}	V_{CCA}
M8	I/O	I/O	I/O
M9	I/O	I/O	I/O
M10	I/O	I/O	I/O
M11	I/O	I/O	I/O
M12	I/O	I/O	I/O

Note: *This V_{CCI} pin may optionally be connected to V_{CCA} if the LP pin is not being used.*

180-Pin CSP (Top View)



180-Pin CSP

Pin Number	eX256 Function
A1	I/O
A2	I/O
A3	GND
A4	NC
A5	NC
A6	NC
A7	NC
A8	NC
A9	NC
A10	NC
A11	NC
A12	I/O
A13	I/O
A14	I/O
B1	I/O
B2	I/O
B3	TCK, I/O
B4	V_{CCI}
B5	I/O
B6	I/O
B7	V_{CCA}
B8	I/O
B9	I/O
B10	V_{CCI}
B11	I/O
B12	I/O
B13	I/O
B14	I/O
C1	I/O
C2	TMS
C3	I/O
C4	I/O
C5	I/O
C6	I/O
C7	PRA, I/O
C8	CLKB
C9	I/O
C10	I/O
C11	I/O
C12	GND
C13	I/O
C14	I/O
D1	I/O
D2	I/O
D3	TDI, I/O
D4	I/O
D5	I/O
D6	I/O
D7	CLKA
D8	I/O
D9	I/O
D10	I/O
D11	I/O
D12	I/O
D13	I/O
D14	I/O
E1	I/O
E2	I/O
E3	I/O
E4	I/O
E5	I/O
E6	I/O
E7	GND
E8	I/O
E9	GND
E10	I/O
E11	I/O
E12	I/O
E13	V_{CCI}
E14	I/O
F1	I/O
F2	I/O
F3	V_{CCI}
F4	I/O
F5	GND
F10	GND
F11	I/O
F12	GND, LP
F13	V_{CCA}
F14	I/O
G1	V_{CCA}
G2	I/O
G3	I/O
G4	I/O
G5	I/O
G10	GND
G11	I/O
G12	I/O
G13	I/O
G14	V_{CCA}
H1	I/O
H2	I/O
H3	TRST, I/O
H4	I/O
H5	GND
H10	GND
H11	I/O
H12	I/O
H13	I/O
H14	I/O
J1	I/O
J2	GND
J3	I/O
J4	V_{CCI}
J5	GND
J10	I/O
J11	V_{CCI}
J12	V_{CCI}*
J13	I/O
J14	I/O
K1	I/O
K2	V_{CCI}*
K3	I/O
K4	V_{CCI}
K5	I/O
K6	I/O
K7	I/O
K8	GND
K9	I/O
K10	GND
K11	I/O
K12	I/O
K13	I/O
K14	I/O
L1	I/O
L2	I/O
L3	I/O
L4	I/O
L5	I/O
L6	I/O
L7	PRB, I/O
L8	HCLK
L9	I/O
L10	I/O
L11	I/O
L12	TDO, I/O
L13	I/O
L14	I/O
M1	I/O
M2	I/O
M3	I/O
M4	I/O
M5	I/O
M6	I/O
M7	I/O
M8	I/O
M9	I/O
M10	I/O
M11	I/O
M12	I/O
M13	V_{CCI}
M14	I/O
N1	I/O
N2	GND
N3	I/O
N4	I/O
N5	I/O
N6	I/O
N7	I/O
N8	V_{CCA}
N9	I/O
N10	I/O
N11	I/O
N12	I/O
N13	I/O
N14	I/O
P1	I/O
P2	I/O
P3	I/O
P4	NC
P5	NC
P6	NC
P7	NC
P8	NC
P9	NC
P10	NC
P11	NC
P12	GND
P13	I/O
P14	I/O

Note: *This V_{CCI} pin may optionally be connected to V_{CCA} if the LP pin is not being used.*

List of Changes

The following table lists critical changes that were made in the current version of the document.

Previous version	Changes in current version (Advanced v0.3)	Page
Advanced v0.2	The Mechanical Drawings section has been removed from the data sheet. The mechanical drawings are now contained in a separate document, "Package Characteristics and Mechanical Drawings," available on the Actel web site.	
	A new section describing Clock Resources has been added.	page 5
	A new table describing I/O Features has been added.	page 5
	The Pin Description section has been updated and clarified.	page 18
	The original Electrical Specifications table was separated into two tables (2.5V and 3.3/5.0V). In both tables, several different currents are specified for V_{OH} and V_{OL}.	Page 8 and 9
	A new table listing 2.5V low power specifications and associated power graphs were added.	page 9
	Pin functions for eX256 TQ100 have been added to the 100-TQFP table.	page 22
	A CS49 pin drawing and pin assignment table including eX64 and eX128 pin functions have been added.	page 23
	A CS128 pin drawing and pin assignment table including eX64, eX128, and eX256 pin functions have been added.	page 24 to page 26
	A CS180 pin drawing and pin assignment table for eX256 pin functions have been added.	page 27 and page 28

Data Sheet Categories

In order to provide the latest information to designers, some data sheets are published before data has been fully characterized. These data sheets are marked as "Advanced" or Preliminary" data sheets. The definition of these categories are as follows:

Advanced

The data sheet contains initial estimated information based on simulation, other products, devices, or speed grades. This information can be used as estimates, but not for production.

Preliminary

The data sheet contains information based on simulation and/or initial characterization. The information is believed to be correct, but changes are possible.

Unmarked (production)

The data sheet contains information that is considered to be final.

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