BINARY COUNTER DESIGN (LOGIC LEVEL), 2008/09

Design requirements

1. The counter should count continuously in a loop from its minimum value to its maximum value or from its maximum value to its minimum value, according to the table below.
2. The output should be in NBC (Natural Binary Code).
3. Internal states should be the same as the output states (no additional encoding/decoding).
4. The design should ensure that the counter does not get stuck in any of the unused states. There is no precise behaviour required in this case, including after reset (0000).
5. T-type flip-flops should be used.
6. NAND and NOR gates should be used in first place (as opposed to AND and OR gates).

How you should proceed (and what you should show in your report)

1. Draw the state graph with unused states left unconnected.
2. Fill in the truth table for the system.
3. Minimize Boolean functions for T3..T0 using Karnaugh maps. Make proper use of the unused states.
4. Check if no loop involving the unused states has been generated during minimization. There should now be a path from any of the unused states to a state belonging to the normal operation loop (not necessarily the minimum or the maximum one). Make changes to the equations if necessary.
5. Using De Morgan's laws, transform your equations so as NAND and NOR gates can be used (except when you can justify that this wouldn't be optimal in your case).
6. Draw the digital circuit schematic (flip-flops and gates) that corresponds to the equations.

Counter parameters

Acct. No.	Limits and Direction
25	3→13
26	14→3
27	14→6
28	14→5
31	4→14
32	4→13
33	5→14
34	3→12
35	12→3
36	13→3
37	14→4
39	3→14
40	13→4