Microelectronics Laboratory

Tasks and Assessment, summer semester 2008/09

Tasks and Due Reports

1. CMOS transistors and circuits with PSpice

Simulation results (plots, waveforms) and their analysis, i.e. observations and theoretical justification.

Precisely:

(a) output and transfer characteristics, 2 NMOSes compared in one plot;

(b) output and transfer characteristics, NMOS and PMOS compared in one plot (at least output chars.), regions of operation;

(c) output and transfer characteristics as function of T, $I_{D(max)}$ as function of W and L, for NMOS and for PMOS;

(d) CMOS inverter static transfer characteristics and supply current characteristics for different k_W, plot for V_{inv}, optimal k_W ;

(e) CMOS inverter dynamic switching waveforms for different k_W, plot for t_{dLH} and t_{dHL}, optimal k_W;

(f) CMOS inverter switching waveforms as function of V_{DD}, T, and load with plots for t_{dLH} and t_{dHL}.

2. Counter design, pre-layout

Your work shown according to the document entitled "Binary Counter Design (Logic Level)." Enclose logical circuit schematic and simulation results from DSch that prove proper operation.

Note. Use your own design parameters—see the PDF.

3. Ring oscillator

An exemplary mask layout and waveforms (for any chosen number of inverters). Measurements of f_{osc}, P for $N = 3; 5; 7; 9$: numeric results; calculation of t_d; plots; analysis and explanation of parameter dependence on number of inverters; analysis and explanation of parameter changes with technology.

Note. Use the technologies given for you as Primary Technology and Second Technology. Don't change anything in your design but technology!

4. Gates: NOT, NAND, NOR, XOR, TG (optimised and standardised cells)

Final mask layout file name and location; electrical schematic; truth table; simulation results proving proper operation (all) and showing equality of delay times (NOT, NAND, and NOR only); comments on your design work (including transistor sizing) and on your results.

Note. Use the technology given for you as Primary Technology.

Note 2. A truth table is a table that tells what should appear on the output(s) for any input(s) possible. Use "X" for "any" and "Z" for "high impedance".

5. Flip-flops: master-slave D, D-based T (transmission gate-based circuits, synchronous reset, standardised cells)

Final mask layout file name and location; logical schematic; function table; simulation results proving proper operation; comments on your design work and on your results.

Note. Use the technology given for you as Primary Technology.

Note 2. A function table is a table that tells what should appear on the output(s) for any input(s) and previous output(s) possible. Use "X" for "any". Use "↑" & "↓" for clock edges.

Note 3. Transistor sizes in all the particular gates should be optimal as determined in Task 4.

6. Counter project, post-layout (implementing the logical circuit from Task 2 and employing adequate standardised cells from Tasks 4 & 5)

Final mask layout file name and location; simulation results proving proper operation; comments on your desing work and on your results.

Note. Use the technology given for you as Primary Technology.

Note 2. Use your gate and flip-flop cells as you designed them; don't change anything! They should just be assembled and connected in this task.

Grading

Component	Report 1	Design & Report 2	Design & Report 3	Designs & Report 4	Designs & Report 5	Design & Report 6	Test 1	Test 2	**Total**
Max. points	10	7	7	25	16	15	10	10	**100**

Evaluation of Microwind Designs (Tasks 4, 5 & 6)

For these tasks the scores above are awarded for:

1. Mask layout
   - (a) Proper operation (proved—see 2(b); including symmetrical delays for NOT, NAND, and NOR) * 5%
   - (b) Masks conforming to the schematic given in 2(a) and not violating design rules (also after *any* two cells are put together in *any* way allowed) * 10%
   - (c) Minimised space consumption within the imposed design constraints (maximised space utilization and optimal distribution of particular elements/cells) 10%
   - (d) Observance of standardisation guidelines 10%
   - (e) Properly designed (material, layer, width) and possibly short interconnections 10%
   - (f) General order and tidiness; clear and consistent description of signals and elements (text, tables, schematics, masks, waveforms) 5%
2. Report
   - (a) Circuit schematic & function definition (except for Task 6 where this is found in Task 2) 10%
   - (b) Simulation results proving proper operation according to the task description and to the function definition given in (a) 15%
   - (c) Measurement results (compulsory are the delay times for NOT, NAND, and NOR) and other numerical parameters describing your design (e.g. space consumption) 10%
   - (d) Comments on design work and on the results obtained 15%

Note. If any of the criteria marked with an asterisk is not fulfilled, the whole design is failed and scored 0 pts.

Note 2. Circuit operation is assessed for your Primary Technology.

Note 3. For Task 6, in part 1, 5% is replaced by 10% and 10% is replaced by 15%; in part 2, (a) does not apply and other scores are consequently reduced.

Note 4. Criteria 1(a)—(c) and 1(e)—(f) also apply to Task 3 but are not scored separately.