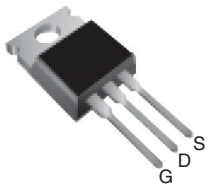
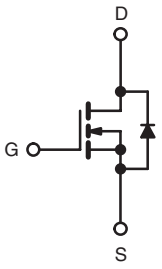
Power MOSFET

PRODUCT SUMMARY		
V_{DS} (V)	100	
$R_{DS(on)}$ (Ω)	V_{GS} = 5.0 V	0.077
Q_g (Max.) (nC)	64	
Q_{gs} (nC)	9.4	
Q_{gd} (nC)	27	
Configuration	Single	

TO-220





N-Channel MOSFET

FEATURES

- Dynamic dV/dt Rating
- Repetitive Avalanche Rated
- Logic-Level Gate Drive
- $R_{DS(on)}$ Specified at V_{GS} = 4 V and 5 V
- 175 °C Operating Temperature
- Fast Switching
- Ease of Paralleling
- Lead (Pb)-free Available

Available

RoHS* COMPLIANT

DESCRIPTION

Third generation Power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The TO-220 package is universally preferred for all commercial-industrial applications at power dissipation levels to approximately 50 W. The low thermal resistance and low package cost of the TO-220 contribute to its wide acceptance throughout the industry.

ORDERING INFORMATION	
Package	TO-220
Lead (Pb)-free	IRL540PbF
	SiHL540-E3
SnPb	IRL540
	SiHL540

ABSOLUTE MAXIMUM RATINGS T_C = 25 °C, unless otherwise noted

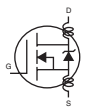
PARAMETER			SYMBOL	LIMIT	UNIT
Drain-Source Voltage			V_{DS}	100	V
Gate-Source Voltage			V_{GS}	± 10	
Continuous Drain Current	V_{GS} at 5.0 V	T_C = 25 °C	I_D	28	A
		T_C = 100 °C		20	
Pulsed Drain Current[a]			I_{DM}	110	
Linear Derating Factor				1.0	W/°C
Single Pulse Avalanche Energy[b]			E_{AS}	440	mJ
Avalanche Current[a]			I_{AR}	28	A
Repetitive Avalanche Energy[a]			E_{AR}	15	mJ
Maximum Power Dissipation	T_C = 25 °C		P_D	150	W
Peak Diode Recovery dV/dt[c]			dV/dt	5.5	V/ns
Operating Junction and Storage Temperature Range			T_J, T_{stg}	- 55 to + 175	°C
Soldering Recommendations (Peak Temperature)	for 10 s			300[d]	
Mounting Torque	6-32 or M3 screw			10	lbf · in
				1.1	N · m

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
b. V_{DD} = 25 V, starting T_J = 25 °C, L = 841 µH, R_G = 25 Ω, I_{AS} = 28 A (see fig. 12c).
c. $I_{SD} \leq$ 28 A, dI/dt ≤ 170 A/µs, $V_{DD} \leq V_{DS}$, $T_J \leq$ 175 °C.
d. 1.6 mm from case.

* Pb containing terminations are not RoHS compliant, exemptions may apply

THERMAL RESISTANCE RATINGS				
PARAMETER	**SYMBOL**	**TYP.**	**MAX.**	**UNIT**
Maximum Junction-to-Ambient	R_{thJA}	-	62	°C/W
Case-to-Sink, Flat, Greasd Surface	R_{thCS}	0.50	-	
Maximum Junction-to-Case (Drain)	R_{thJC}	-	1.0	

SPECIFICATIONS T_J = 25 °C, unless otherwise noted							
PARAMETER	**SYMBOL**	**TEST CONDITIONS**		**MIN.**	**TYP.**	**MAX.**	**UNIT**
Static							
Drain-Source Breakdown Voltage	V_{DS}	V_{GS} = 0 V, I_D = 250 µA		100	-	-	V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to 25 °C, I_D = 1 mA		-	0.12	-	V/°C
Gate-Source Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA		1.0	-	2.0	V
Gate-Source Leakage	I_{GSS}	V_{GS} = ± 10 V		-	-	± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 100 V, V_{GS} = 0 V		-	-	25	µA
		V_{DS} = 80 V, V_{GS} = 0 V, T_J = 150 °C		-	-	250	
Drain-Source On-State Resistance	$R_{DS(on)}$	V_{GS} = 5.0 V	I_D = 17 A[b]	-	-	0.077	Ω
		V_{GS} = 4.0 V	I_D = 14 A[b]	-	-	0.11	
Forward Transconductance	g_{fs}	V_{DS} = 50 V, I_D = 17 A		12	-	-	S
Dynamic							
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1.0 MHz, see fig. 5		-	2200	-	pF
Output Capacitance	C_{oss}			-	560	-	
Reverse Transfer Capacitance	C_{rss}			-	140	-	
Total Gate Charge	Q_g	V_{GS} = 5.0 V	I_D = 28 A, V_{DS} = 80 V, see fig. 6 and 13[b]	-	-	64	nC
Gate-Source Charge	Q_{gs}			-	-	9.4	
Gate-Drain Charge	Q_{gd}			-	-	27	
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 50 V, I_D = 28 A, R_G = 9.0 Ω, R_D = 1.7 Ω, see fig. 10[b]		-	8.5	-	ns
Rise Time	t_r			-	170	-	
Turn-Off Delay Time	$t_{d(off)}$			-	35	-	
Fall Time	t_f			-	80	-	
Internal Drain Inductance	L_D	Between lead, 6 mm (0.25") from package and center of die contact 		-	4.5	-	nH
Internal Source Inductance	L_S			-	7.5	-	
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I_S	MOSFET symbol showing the integral reverse p - n junction diode 		-	-	28	A
Pulsed Diode Forward Current[a]	I_{SM}			-	-	110	
Body Diode Voltage	V_{SD}	T_J = 25 °C, I_S = 28 A, V_{GS} = 0 V[b]		-	-	2.5	V
Body Diode Reverse Recovery Time	t_{rr}	T_J = 25 °C, I_F = 28 A, dI/dt = 100 A/µs[b]		-	200	260	ns
Body Diode Reverse Recovery Charge	Q_{rr}			-	1.7	2.90	µC
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L_S and L_D)					

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).

b. Pulse width ≤ 300 µs; duty cycle ≤ 2 %.

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

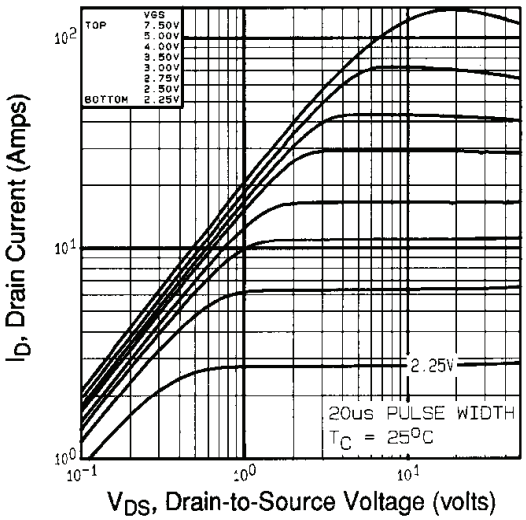


Fig. 1 - Typical Output Characteristics, T_C = 25 °C

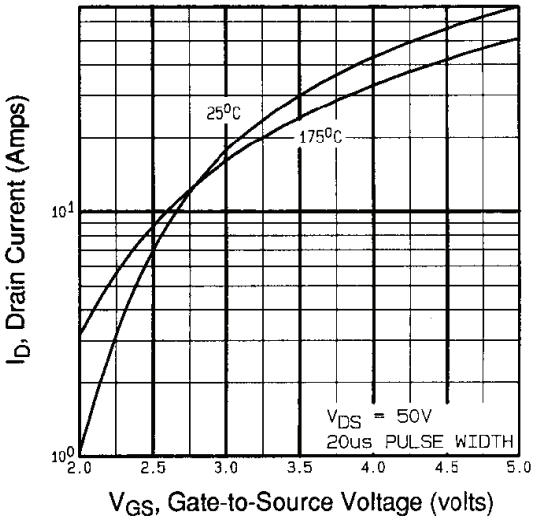


Fig. 3 - Typical Transfer Characteristics

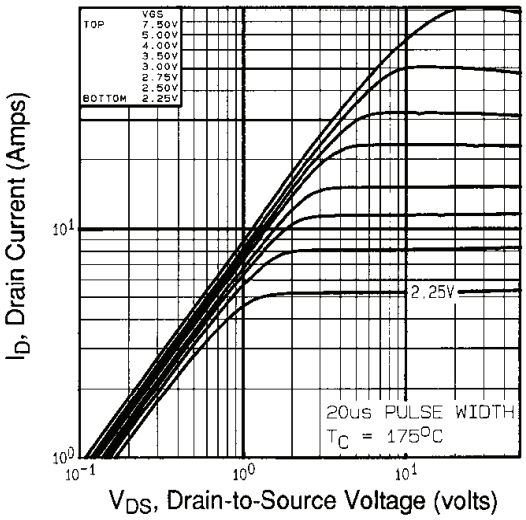


Fig. 2 - Typical Output Characteristics, T_C = 175 °C

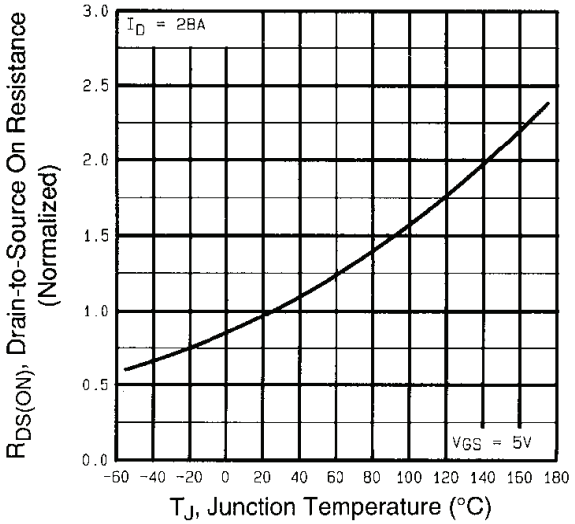


Fig. 4 - Normalized On-Resistance vs. Temperature

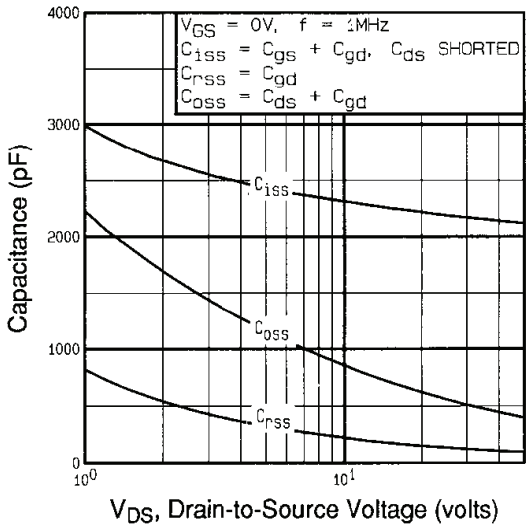


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

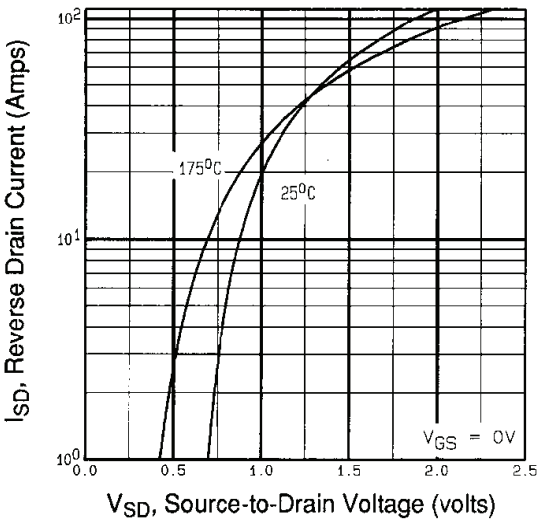


Fig. 7 - Typical Source-Drain Diode Forward Voltage

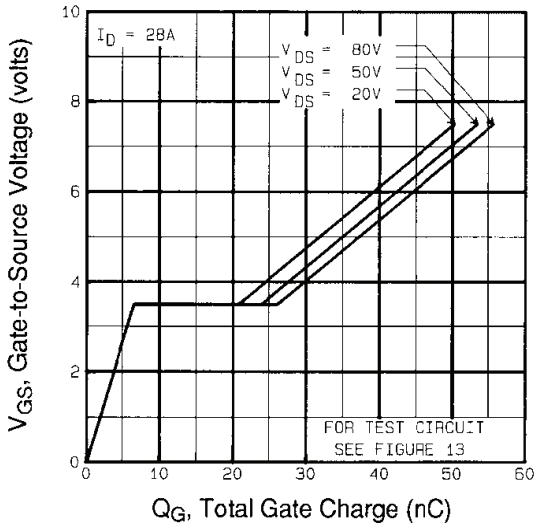


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

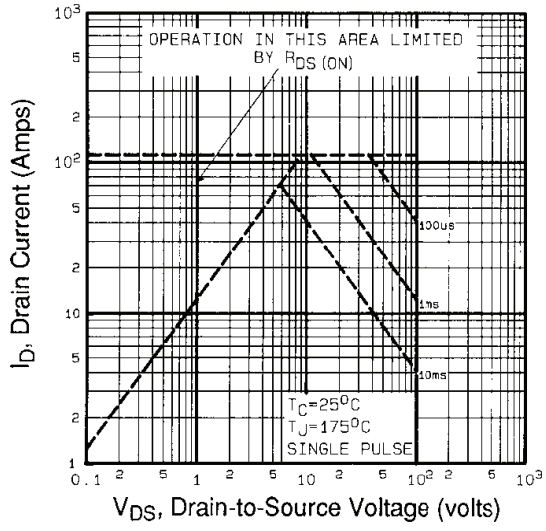


Fig. 8 - Maximum Safe Operating Area

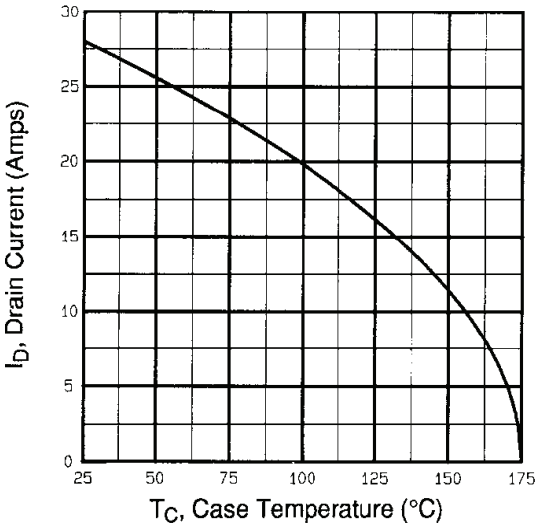


Fig. 9 - Maximum Safe Operating Area

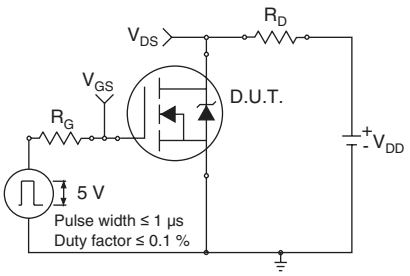


Fig. 10a - Switching Time Test Circuit

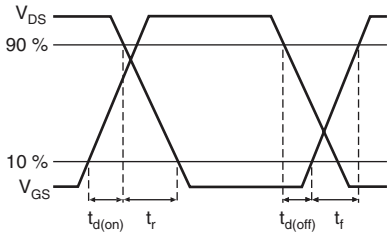


Fig. 10b - Switching Time Waveforms

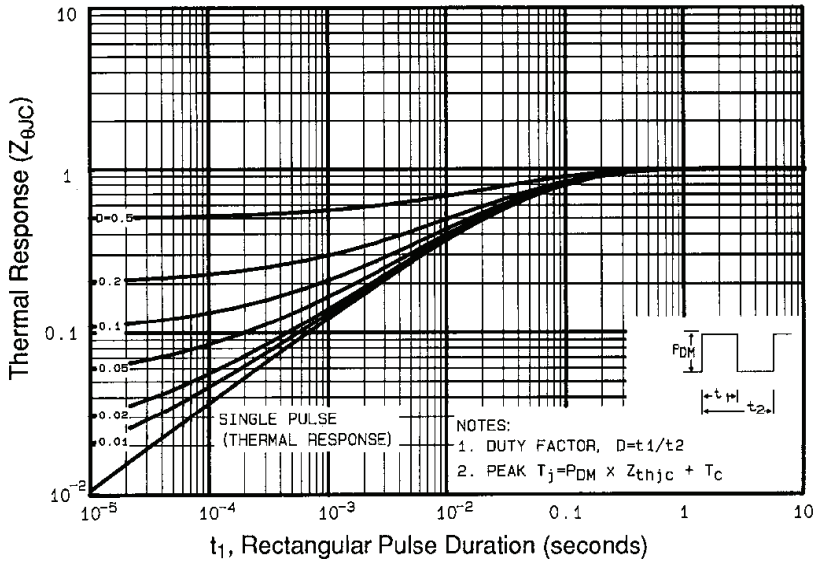


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

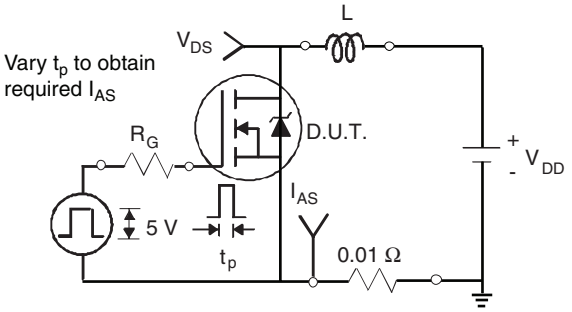


Fig. 12a - Unclamped Inductive Test Circuit

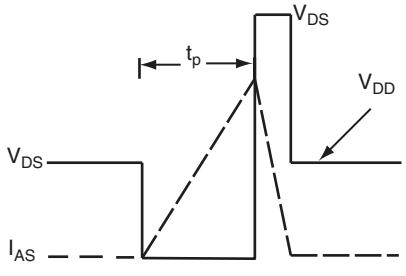


Fig. 12b - Unclamped Inductive Waveforms

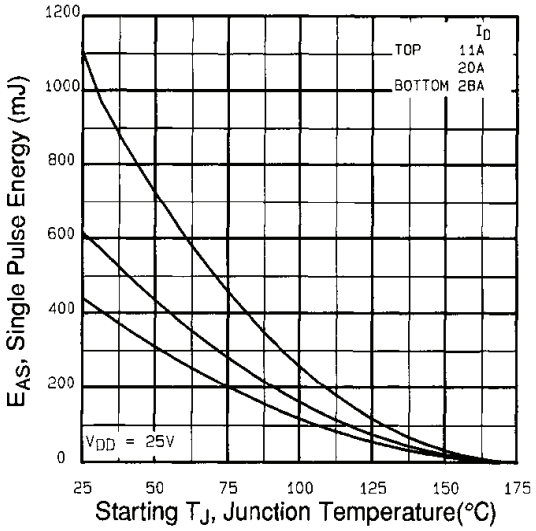


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

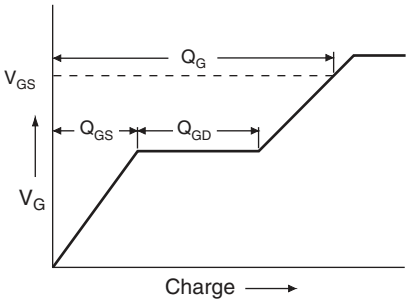


Fig. 13a - Basic Gate Charge Waveform

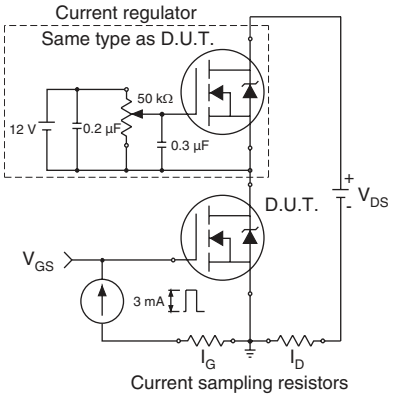
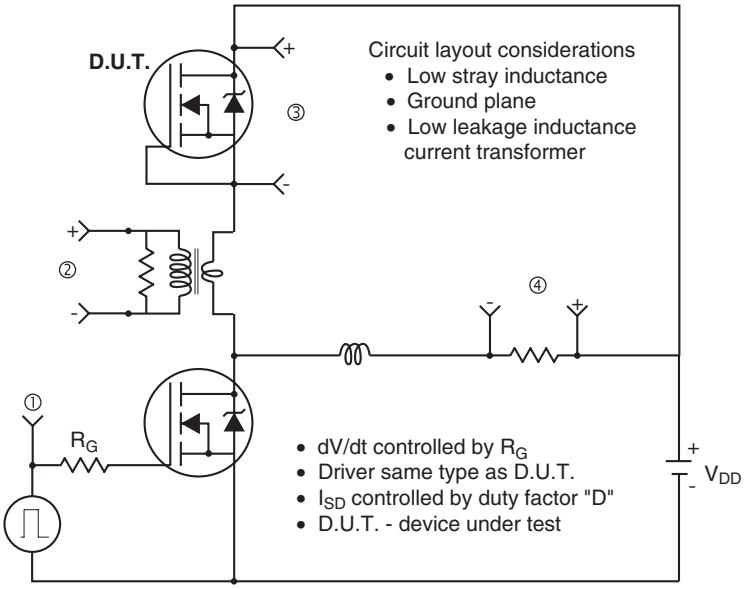
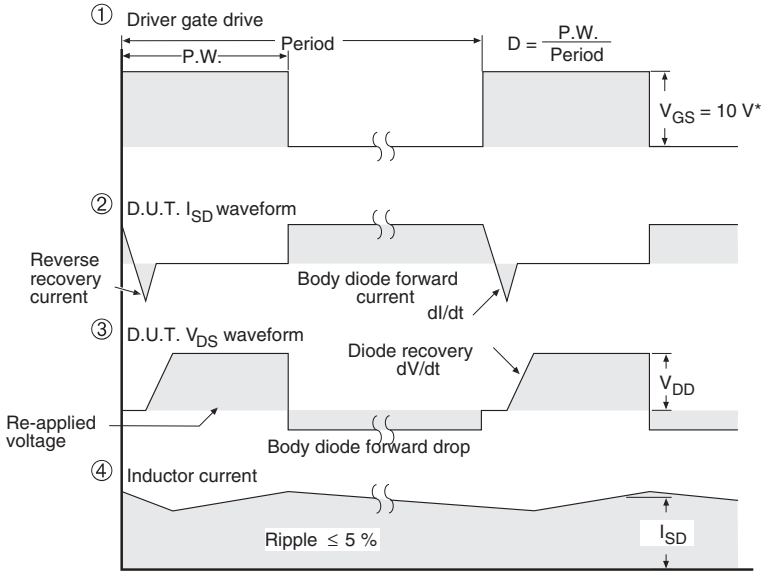


Fig. 13b - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit





* V_{GS} = 5 V for logic level devices

Fig. 14 - For N-Channel

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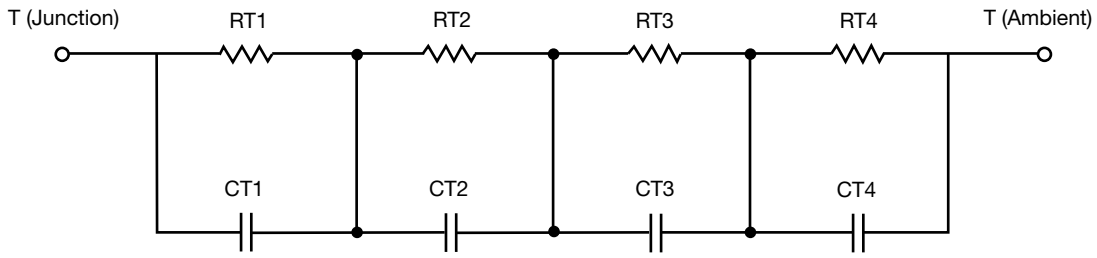
R-C Thermal Model Parameters

DESCRIPTION

The parametric values in the R-C thermal model have been derived using curve-fitting techniques. R-C values for the electrical circuit in the Foster/tank and Cauer/filter configurations are included. When implemented in P-SPICE, these values have matching characteristic curves to the single-pulse transient thermal impedance curves for the MOSFET.

These RC values can be used in the P-SPICE simulation to evaluate the thermal behavior of the MOSFET junction temperature under a defined power profile. These techniques are described in application note AN609, “Thermal Simulation of Power MOSFETs on the P-SPICE Platform”.

R-C THERMAL MODEL FOR TANK CONFIGURATION

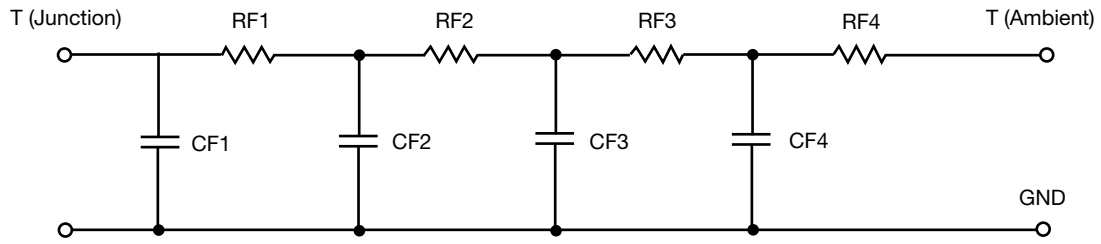


R-C VALUES FOR TANK CONFIGURATION			
THERMAL RESISTANCE (°C/W)			
Junction to	**Ambient**	**Case**	**Foot**
RT1	N/A	206.9037m	N/A
RT2	N/A	395.9929m	N/A
RT3	N/A	227.3703m	N/A
RT4	N/A	170.3629m	N/A
THERMAL CAPACITANCE (Joules/°C)			
Junction to	**Ambient**	**Case**	**Foot**
CT1	N/A	221.9978m	N/A
CT2	N/A	62.2678m	N/A
CT3	N/A	371.7813m	N/A
CT4	N/A	5.4775m	N/A

Note
N/A indicates not applicable

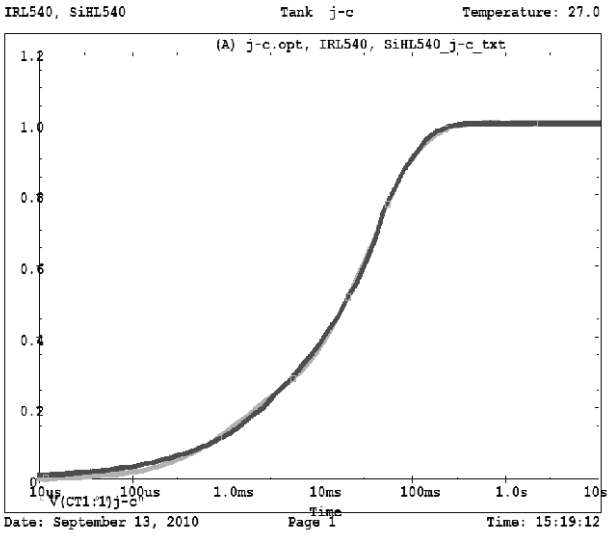
This document is intended as a SPICE modeling guideline and does not constitute a commercial product datasheet. Designers should refer to the appropriate datasheet of the same number for guaranteed specification limits.

R-C THERMAL MODEL FOR FILTER CONFIGURATION



R-C VALUES FOR FILTER CONFIGURATION			
THERMAL RESISTANCE (°C/W)			
Junction to	**Ambient**	**Case**	**Foot**
RF1	N/A	216.4514m	N/A
RF2	N/A	296.1503m	N/A
RF3	N/A	285.9659m	N/A
RF4	N/A	200.8331m	N/A
THERMAL CAPACITANCE (Joules/°C)			
Junction to	**Ambient**	**Case**	**Foot**
CF1	N/A	5.5720m	N/A
CF2	N/A	27.3086m	N/A
CF3	N/A	53.6821m	N/A
CF4	N/A	13.2668m	N/A

Note
N/A indicates not applicable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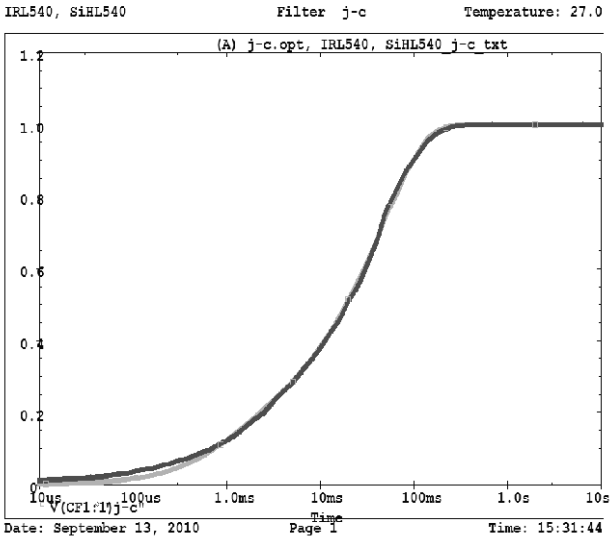
0.2
0
10us
100us
1.0ms
10ms
100ms
1.0s
10s
V(CT1:1)j-c
Time
Date: September 13, 2010
Page 1
Time: 15:19:12


IRL540, SiHL540
Filter j-c
Temperature: 27.0
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1.0
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0.6
0.4
0.2
0
10us
100us
1.0ms
10ms
100ms
1.0s
10s
V(CF1:1)j-c
Time
Date: September 13, 2010
Page 1
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