

Power MOSFET

PRODUCT SUMMARY

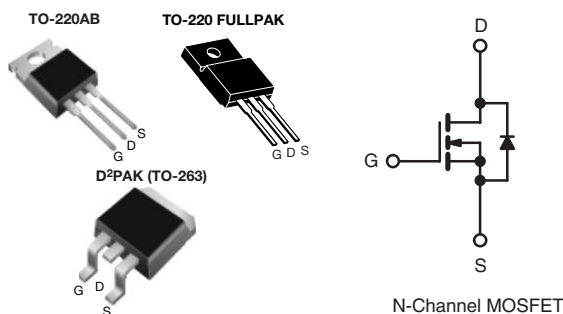
V_{DS} (V) at T_J max.	560 V	
$R_{DS(on)}$ (Ω)	$V_{GS} = 10$ V	0.38
Q_g (Max.) (nC)	68	
Q_{gs} (nC)	17.6	
Q_{gd} (nC)	21.8	
Configuration	Single	

FEATURES

- Low Figure-of-Merit $R_{on} \times Q_g$
- 100 % Avalanche Tested
- Gate Charge Improved
- T_{rr}/Q_{rr} Improved
- Compliant to RoHS Directive 2002/95/EC



Available
RoHS*
COMPLIANT



ORDERING INFORMATION

Package	TO-220AB	D ² PAK (TO-263)	TO-220 FULLPAK
Lead (Pb)-free	SiHP16N50C-E3	SiHB16N50C-E3	SiHF16N50C-E3

ABSOLUTE MAXIMUM RATINGS $T_C = 25$ °C, unless otherwise noted

PARAMETER			SYMBOL	LIMIT		UNIT
				TO220-AB D ² PAK (TO-263)	TO-220 FULLPAK	
Drain-Source Voltage			V _{DS}	500		V
Gate-Source Voltage			V _{GS}	± 30		
Continuous Drain Current (T _J = 150 °C) ^a	V _{GS} at 10 V	T _C = 25 °C	I _D	16		A
		T _C = 100 °C		10		
Pulsed Drain Current ^c			I _{DM}	40		
Linear Derating Factor				2		
Single Pulse Avalanche Energy ^b			E _{AS}	320		mJ
Maximum Power Dissipation			P _D	250	38	W
Operating Junction and Storage Temperature Range			T _J , T _{stg}	- 55 to + 150		°C
Soldering Recommendations (Peak Temperature) ^d	for 10 s			300		

Notes

- Limited by maximum junction temperature.
- $V_{DD} = 50$ V, starting $T_J = 25$ °C, $L = 2.5$ mH, $R_g = 25$ Ω , $I_{AS} = 16$ A.
- Repetitive rating; pulse width limited by maximum junction temperature.
- 1.6 mm from case.

* Pb containing terminations are not RoHS compliant, exemptions may apply

THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	TO220-AB D ² PAK (TO-263)	TO-220 FULLPAK	UNIT
Maximum Junction-to-Ambient	R_{thJA}	62	65	°C/W
Maximum Junction-to-Case (Drain)	R_{thJC}	0.5	3.3	
Junction-to-Ambient (PCB mount) ^a	R_{thJA}	40	-	

Note

a. When mounted on 1" square PCB (FR-4 or G-10 material).

SPECIFICATIONS $T_J = 25\text{ °C}$, unless otherwise noted

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}$, $I_D = 250\text{ }\mu\text{A}$	500	-	-	V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to 25 °C , $I_D = 1\text{ mA}$	-	0.6	-	V/°C
Gate-Source Threshold Voltage (N)	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	3.0	-	5.0	V
Gate-Source Leakage	I_{GSS}	$V_{GS} = \pm 30\text{ V}$	-	-	± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 500\text{ V}$, $V_{GS} = 0\text{ V}$	-	-	50	μA
		$V_{DS} = 400\text{ V}$, $V_{GS} = 0\text{ V}$, $T_J = 125\text{ °C}$	-	-	250	
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$, $I_D = 8\text{ A}$	-	0.31	0.38	Ω
Forward Transconductance ^a	g_{fs}	$V_{DS} = 50\text{ V}$, $I_D = 3\text{ A}$	-	3	-	S
Dynamic						
Input Capacitance	C_{iss}	$V_{GS} = 0\text{ V}$, $V_{DS} = 25\text{ V}$, $f = 1.0\text{ MHz}$	-	1900	-	pF
Output Capacitance	C_{oss}		-	230	-	
Reverse Transfer Capacitance	C_{rss}		-	24	-	
Total Gate Charge	Q_g	$V_{GS} = 10\text{ V}$, $I_D = 16\text{ A}$, $V_{DS} = 400\text{ V}$	-	45	68	nC
Gate-Source Charge	Q_{gs}		-	18	-	
Gate-Drain Charge	Q_{gd}		-	22	-	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 250\text{ V}$, $I_D = 16\text{ A}$, $R_g = 9.1\text{ }\Omega$, $V_{GS} = 10\text{ V}$	-	27	-	ns
Rise Time	t_r		-	156	-	
Turn-Off Delay Time	$t_{d(off)}$		-	29	-	
Fall Time	t_f		-	31	-	
Gate Input Resistance	R_g	$f = 1\text{ MHz}$, open drain	-	1.6	-	Ω
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	MOSFET symbol showing the integral reverse p - n junction diode 	-	-	16	A
Pulsed Diode Forward Current	I_{SM}		-	-	30	
Body Diode Voltage	V_{SD}	$T_J = 25\text{ °C}$, $I_S = 10\text{ A}$, $V_{GS} = 0\text{ V}$	-	-	1.8	V
Body Diode Reverse Recovery Time	t_{rr}	$T_J = 25\text{ °C}$, $I_F = I_S$, $dI/dt = 100\text{ A}/\mu\text{s}$, $V_R = 20\text{ V}$	-	555	-	ns
Body Diode Reverse Recovery Charge	Q_{rr}		-	5.5	-	μC
Body Diode Reverse Recovery Current	I_{RRM}		-	18	-	A

Note

- The information shown here is a preliminary product proposal, not a commercial product data sheet. Vishay Siliconix is not committed to produce this or any similar product. This information should not be used for design purposes, nor construed as an offer to furnish or sell such products.

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

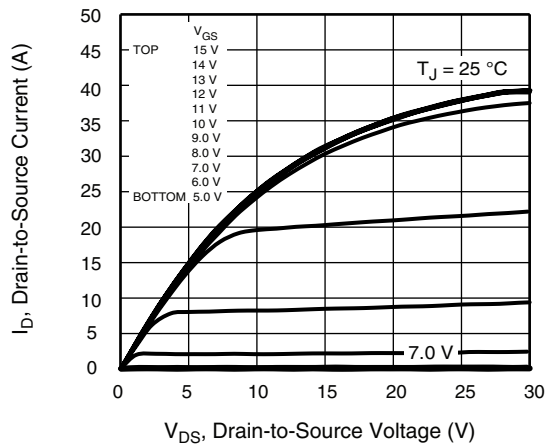


Fig. 1 - Typical Output Characteristics (TO-220)

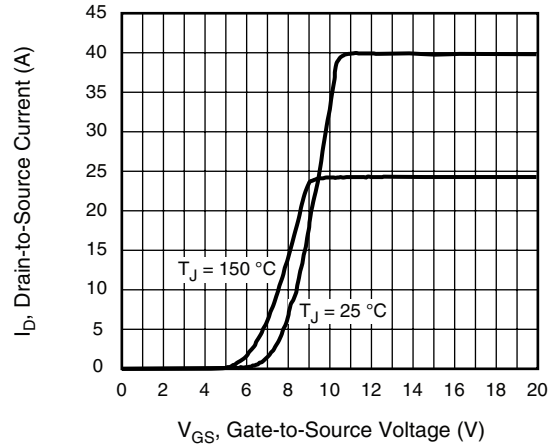


Fig. 3 - Typical Transfer Characteristics

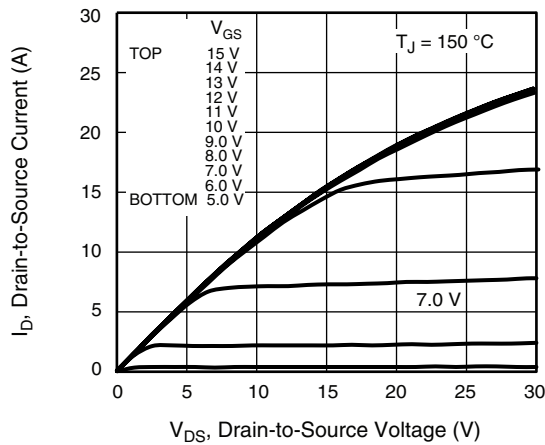


Fig. 2 - Typical Output Characteristics (TO-220)

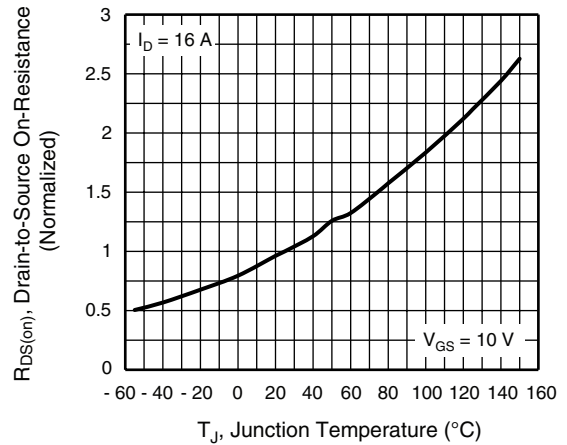


Fig. 4 - Normalized On-Resistance vs. Temperature

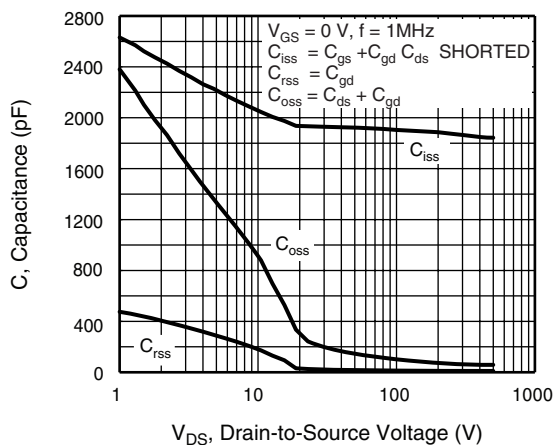


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

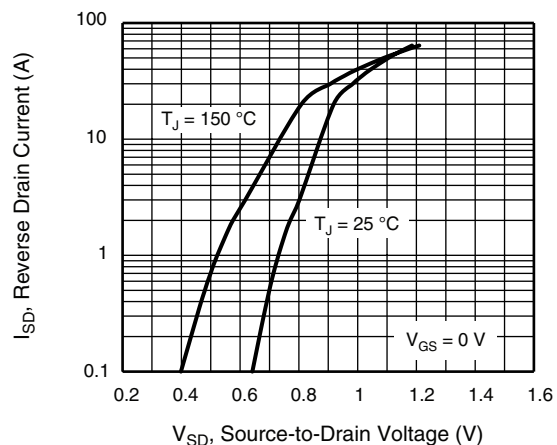


Fig. 7 - Typical Source-Drain Diode Forward Voltage

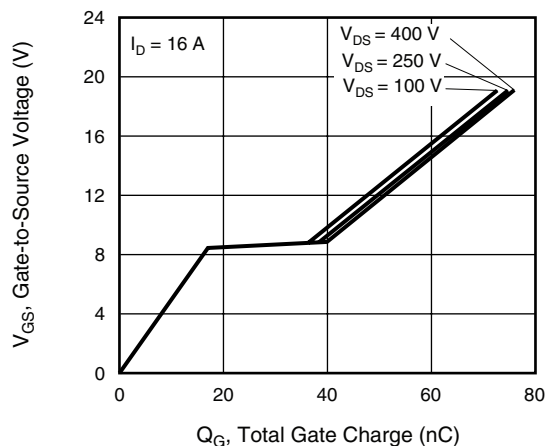


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

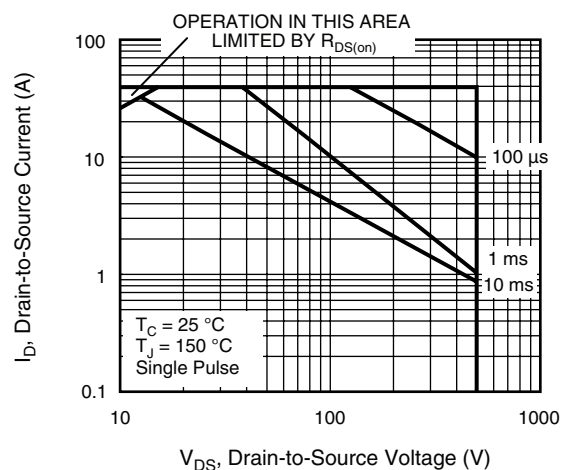


Fig. 8 - Maximum Safe Operating Area (TO-220AB, D²PAK)

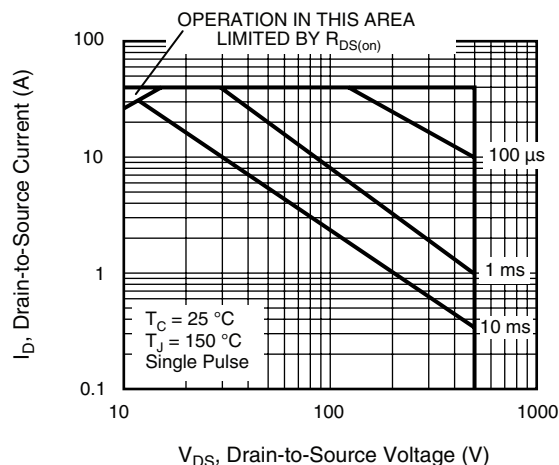


Fig. 9 - Maximum Safe Operating Area (TO-220 FULLPAK)

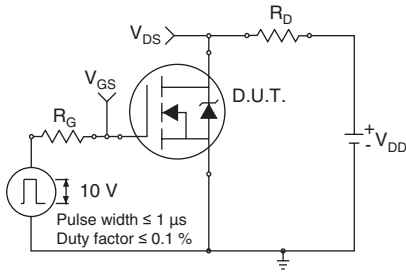


Fig. 10a - Switching Time Test Circuit

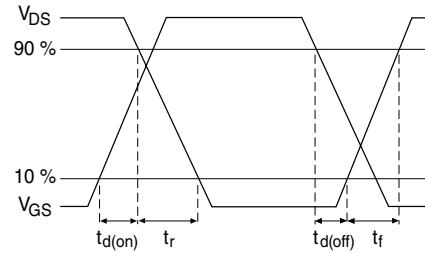


Fig. 10b - Switching Time Waveforms

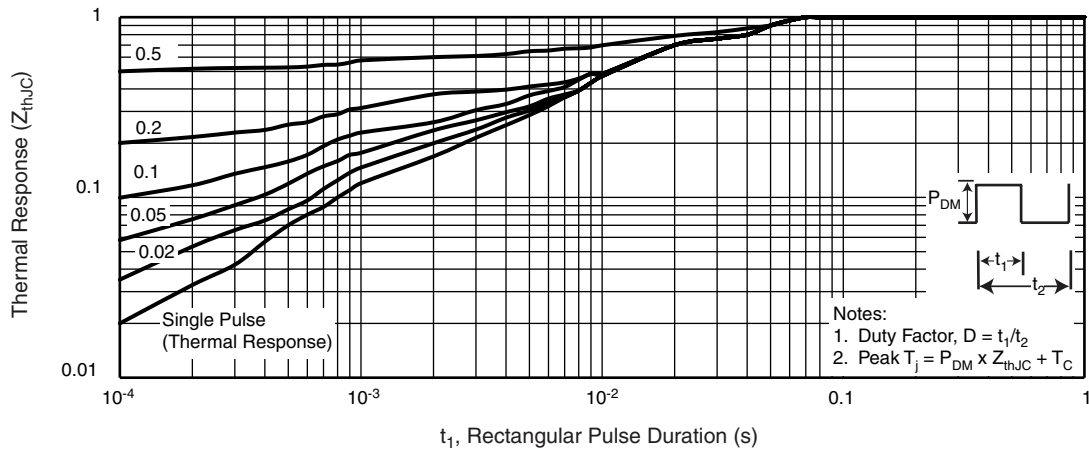


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case (TO-220AB, D²PAK)

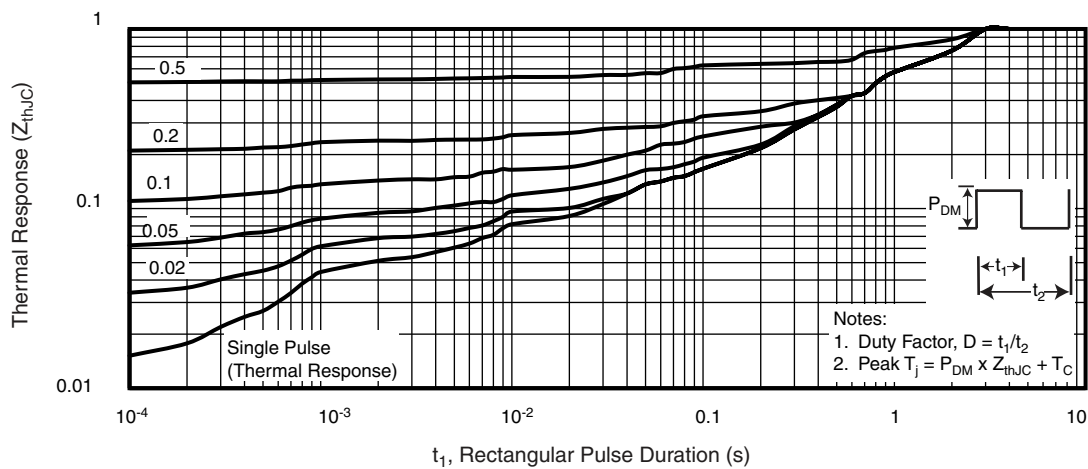


Fig. 12 - Maximum Effective Transient Thermal Impedance, Junction-to-Case (TO-220 FULLPAK)

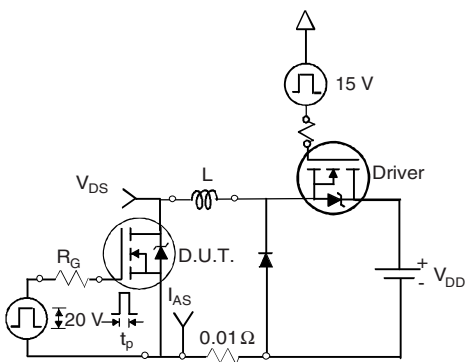


Fig. 13a - Unclamped Inductive Test Circuit

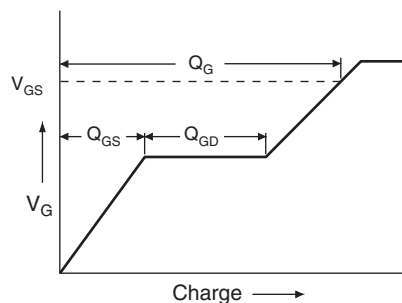


Fig. 14a - Basic Gate Charge Waveform

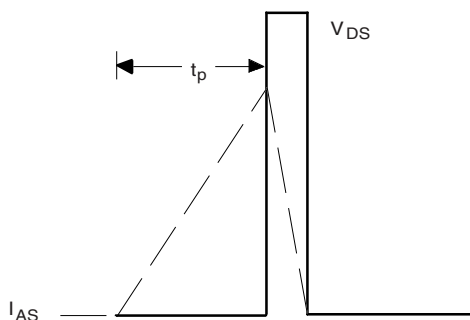


Fig. 13b - Unclamped Inductive Waveforms

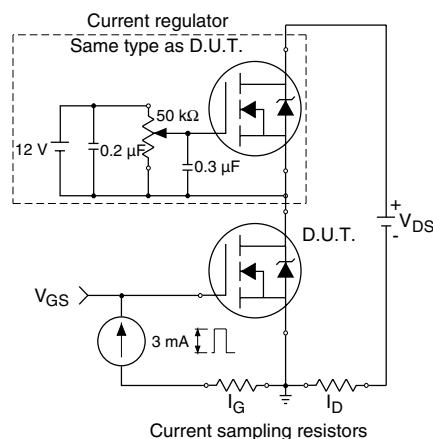
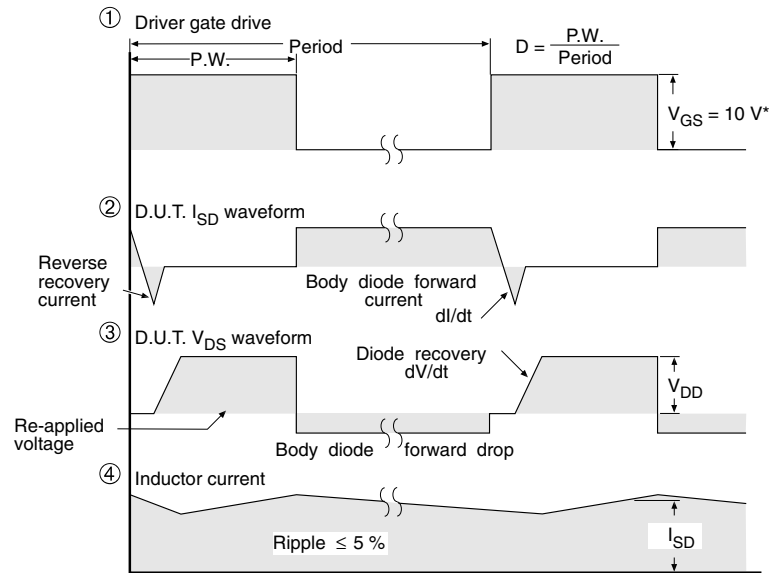
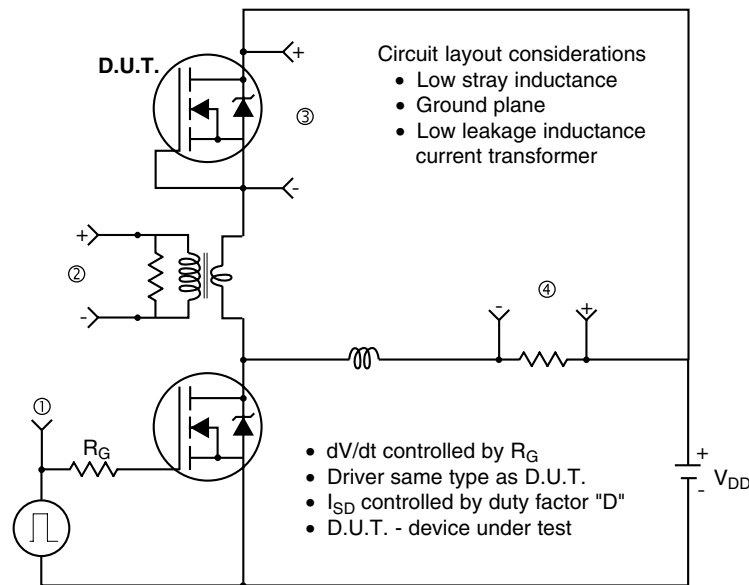


Fig. 14b - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit



* $V_{GS} = 5\text{ V}$ for logic level devices

Fig. 15 - For N-Channel

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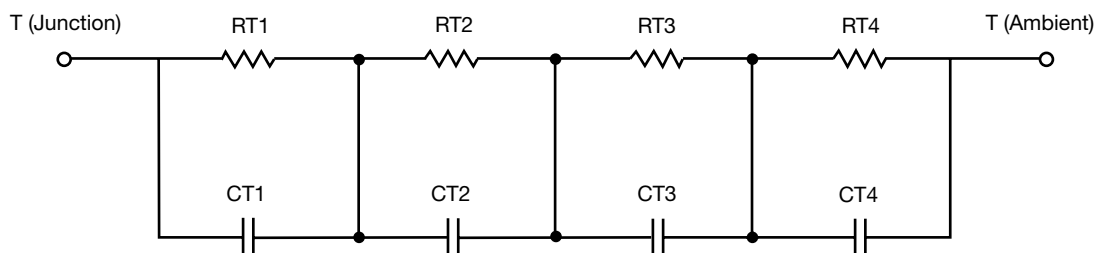
R-C Thermal Model Parameters

DESCRIPTION

The parametric values in the R-C thermal model have been derived using curve-fitting techniques. R-C values for the electrical circuit in the Foster/tank and Cauer/filter configurations are included. When implemented in P-SPICE, these values have matching characteristic curves to the single-pulse transient thermal impedance curves for the MOSFET.

These RC values can be used in the P-SPICE simulation to evaluate the thermal behavior of the MOSFET junction temperature under a defined power profile. These techniques are described in application note AN609, "Thermal Simulation of Power MOSFETs on the P-SPICE Platform".

R-C THERMAL MODEL FOR TANK CONFIGURATION

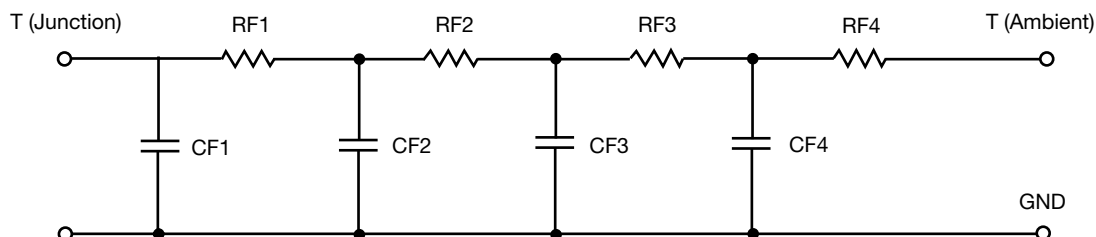


R-C VALUES FOR TANK CONFIGURATION			
THERMAL RESISTANCE (°C/W)			
Junction to	Ambient	SiHP-SiHB Case	SiHF Case
RT1	N/A	32.3517 m	167.5117 m
RT2	N/A	188.0759 m	1.2673
RT3	N/A	201.3236 m	1.7202
RT4	N/A	78.2488 m	144.9883 m
THERMAL CAPACITANCE (Joules/°C)			
Junction to	Ambient	SiHP-SiHB Case	SiHF Case
CT1	N/A	12.1244 m	82.7807 m
CT2	N/A	135.8367 m	1.0857
CT3	N/A	59.5808 m	731.5658 m
CT4	N/A	336.9463 m	3.3959 m

Note:

1. N/A indicates not applicable
2. Package Names: SiHP..TO220AB, SiHB..D2PAK(TO263), SiHF..TO220 FullPAK

This document is intended as a SPICE modeling guideline and does not constitute a commercial product datasheet. Designers should refer to the appropriate datasheet of the same number for guaranteed specification limits.

R-C THERMAL MODEL FOR FILTER CONFIGURATION**R-C VALUES FOR FILTER CONFIGURATION**

THERMAL RESISTANCE (°C/W)			
Junction to	Ambient	SiHP-SiHB Case	SiHF Case
RF1	N/A	104.6594 m	51.2178 m
RF2	N/A	312.0074 m	134.7475 m
RF3	N/A	5.4260 m	206.4347 m
RF4	N/A	77.9072 m	2.9076
THERMAL CAPACITANCE (Joules/°C)			
Junction to	Ambient	SiHP-SiHB Case	SiHF Case
CF1	N/A	13.9178 m	137.1847 u
CF2	N/A	32.5839 m	10.6770 m
CF3	N/A	50.0700 m	73.0024 m
CF4	N/A	20.0146 m	364.3531 m

Note:

1. N/A indicates not applicable
2. Package Names: SiHP..TO220AB, SiHB..D2PAK(TO263), SiHF..TO220 FullPAK

